"TORA TORA"

COMPUTER SERVICE AND THEORY OF OPERATING MANUAL

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INSTALLATION REQUIREMENTS

1.0 Receiving and Set-Up

"TORA-TORA"---------has been shipped to you pre-tested. The game is ready to play, after removal of the shipping carton. You should, however, perform the following procedures to insure quality performance.

A. Examine the game cabinet for mistreatment during shipping.

B. Examine the interior of the game by opening the back door and inspecting for the following:

1) All connectors should be firmly seated.

2) All integrated circuit packages (IC's) sockets should be firmly seated. (The top row of IC's and the microprocessor are in sockets).

3) The fuse is properly connected and the safety cover is over the top of the AC terminal strip.

4) All loose bolts, washers, screws or other objects should be removed or replaced.

5) Assure that TV monitor is firmly mounted and keyboard panels are well connected.

6) Check the serial number located on the label on the left panel, next to the back door. This number should be entered in the space below, so that your unit is fully identified.

SERIAL NO.____________________

(c) Ensure that your power is at 110V Ac, 60 Hz. The power supply shipped to you is designed to allow ± 10% variation in line voltage.

(d) Ensure that your power has a safety ground and a 3-prong plug is to be used. The safety ground used in your game is to help protect the unit from static shock. A static ground is connected from the front door to the safety ground, to protect the unit and customers from any shock. Spraying the carpet around your unit with a conductive anti-static spray will also protect the unit and provide customer satisfaction. In the event of a shock, the game attempts to repair the damage and continue, but the shock may be so severe, that the game will stop running. If this happens, the game will automatically reset in 16 seconds and restart, but with the loss of all credits.

2.0 Game Adjustments

The game adjustments are discussed in Section 1.3 of the manual. Normally, these adjustments were made at the factory, and the operation of the power supply and monitor will be excellent. In the event that the horizontal hold adjustment should be required, be sure to let the unit warm up for 15 or 20 minutes before final setting of this adjustment.

3.0 Sound Adjustment

If the volume is incorrect for your location, open the back door and adjust the volume controls as described in Section 3.5 of your manual.

4.0 Reset or Tilt Switch

Inside the coin door is a Tilt switch. This provides a reset capability of the front door. In the event that this switch is too sensitive, it may be bent to increase the

required movement before the unit resets with a loss of credit to the customer. This switch has been provided to protect the unit from mistreatment. If it is too sensitive, a customer may lose his credits unjustly, and cause damage.

SECTION 1. GENERAL INFORMATION

1.1 INTRODUCTION

1.1.1 The Purpose-

The purpose of this manual is to provide the user with information which will aid him in solving problems. Sections in this document will be of interest to the operator, repairman, and even the hobbyist. We suggest that you review the outline to evaluate the information that is included in this manual, so that you may use it in future reference.

1.1.2 Basic System Description-

This Air Naval game named "Tora Tora" contains a central processor, memory, input and output devices, just as other digital computers (games) on the market today. This system is composed of both hardware and software. The hardware consists of input and output control logic elements, while the software is what makes the game unique. The software control offers a great many benefits which may or may not be immediately obvious.If deficiencies show up in the new game, these can be worked out in such a way that the software is corrected and shipped to the repair centers at only a fraction of the cost it would take to recall a large number of games, and modify them to correct the problem. Such software systemsare very flexible, for instance, many objects can be moved on the CRT, apparently simultaneously without increasing the system's complexity. This allows this particular game system to be applicable to a large variety of future games.

Another advantage is, once technicians become familiar with this particular microprocessor game system, technicians will be able to repair games, using this system. Since most microprocessor functions are similar, there's a great deal of positive transfer from one system to another. In the following pages, the architecture of the 6800 CPU and memory board will be discussed. In addition, we will discuss the keyboard interfaces and the soundboard operations. Finally, a number of trouble-shooting procedures (approaches) for dealing with problems will be provided. This information, combined with ordinary trouble-shooting equipment, will allow the average video game technician to fully explore the circuitry in this game.

1.2 A Typicial Game Sequence

The Play Mode-

The play mode is entered by pressing the "Start" button. When the game starts, the scoreboard flashes "Enemy Squadron" three times. Then the attack begins. The enemy planes dive out of the sky and drop torpedo bombs. Having dropped their bombs, the planes exit to the left and right, and reunite with the larger enemy squadron. As the planes exit, the bombs fall through the air and upon splashdown travel toward the ships.

This is a fleet of allied ships. The ships are anchored in a harbor and on the coast of the harbor is a track upon which rides a heavy artillery cannon. This is the view point of the player. He sits at the controls, moving the gun left and right, and firing on the attacking planes.

It is the battle between these two forces that develops the action of the game. As the battle proceeds, the torpedoes hit and sink ships, and the shells fired from the guns hit and destroy enemy planes. If the player shoots all the planes out of the sky he receives another fleet of ships and another squadron of enemy planes attacks.

There are only two conditions upon which the game can end:
Either- (1) The players gun is hit 3 times.
Or------(2) All the ships in a given fleet are sunk.

1.3 Electrical Adjustments

1.3.1 Introduction-

In this system, there are four main categories of electrical adjustments, and these are: (1) TV Monitor Adjustment, (2) Power Supply Adjustment, (3) Operator Adjustment, and (4) Sound System Adjustment.

1.3.2 TV Monitor Adjustment-

These adjustments are located on the TV monitor. The four most commonly used ones (A-D) are found accessible from the rear of the monitor. Brightness, contrast,vertical hold, and horizontal linearity are adjusted via hand control pots. Vertical linearity and vertical size are adjusted via pots located on the circuit board in the monitor. The yoke is adjusted at the rear of the picture tube. More detail concerning the location and the operation of the monitor can be found in the monitor service manual and parts catalog.

(A) Horizontal hold-Adjustment is indicated if the picture is off-center horizontally. If the playing field or images appear warped at the top of the screen, or if the picture is

broken up into a series of diagonal lines, adjust for a stable picture. (B) Vertical hold- Adjustment is indicated if the picture is stable but not centered vertically. (C) Brightness- Brightness is adjusted before contrast. Adjust for a light grey background. (D) Contrast- adjust so that the images are as bright as possible against the light grey backgound without being blurred. (E) Vertical Linearity- Adjust only if the images at the right of the CRT appear to be shorter than those on the left. (F) Vertical Height-Adjust if the score area appears to be to far to the right on the screen Caution: Be aware that there are some inner dependents between the vertical linearity and the height adjustment. (G) Horizontal Width- Adjustment is indicated if the score area does not fit onto the screen, adjust the horizontal width until the score and gun are equal distance from the top and bottom. (H) Yoke- Yoke adjustments are indicated only if the entire picture is off center and the horizontal hold adjustment has insufficient effect. Adjust both yoke rings simultaneously, for optimum centering of the image.

1.3.3 <u>Power Supply Adjustments-</u>

The power supply adjustments are performed at two locations within this system. First, on the TV monitor, the input chassis has been designed to operate on any of 3 imput power sources. Before power is applied to the chassis, the top selector should be connected to agree with power input (100V or 120V or 230V AC 50/60 HZ). The top selector is located under a protective cover near the power transformer on the video monitor chassis. The second adjustments are performed at the power supply, PSI. Figure I illustrates the adjustment

locations and the arrows indicate direction of increase. (A) +5.0 Volt Supply- Connect a voltmeter to the power terminal block at the +5 terminal (the bottom terminal) and ground (the middle terminal) and adjust the 5-volt pot for a reading of exactly +5 volts. (B) +12 Volt Supply- Connect a voltmeter to the power terminal marked +12 volts(the 2nd terminal form the bottom) and ground and adjust the 12 volt pot for a reading of exactly +12 volts. (C) -12 Volt Supply- Connect a voltmeter to the -12 volt terminal (the top terminal) and ground and adjust the -12 volt pot for a reading of exactly -12 volts. The power supply also has two primary windings which, when applied in series, allow utilization at 230 volts versus the nominal 115 volts. The adjustment can be made by rewiring the power supply.

1.3.4 <u>Sound System Adjustment-</u>

Volume adjustments are provided for the two independent sound channels within the game. This has been done so that the two sounds may be adjusted to the same general level. The computer within the game, controls the volume of each of the individual sounds and each has been adjusted to provide an over-all effect. To begin to adjust the sound, there are two pots located on the sound board, which adjusts the left and right volumes. The adjustments are illustrated in Figure 3. The arrow indicates the direction of volume increase. These volume controls are effective only if the speakers are plugged directly into the board. When a sound amplifier is provided the amplifier will present a high input impedence, and there-

fore these volume controls are ineffective. The volume controls on the amplifier will control the volume.

1.4 System Architecture

1.4.1 System Sub-Assemblies-

Figure 4 shows the basic electrical sub-assemblies required for the system. The system consists of a power supply which supplies power to the computer and memory board, the button interface board and the sound and keyboard control board. The power supply is connected by a wiring harness. This distributes power to the computer and memory board, and sound and button control board. The player controls are located on an external button panel mounted to the front of the cabinet. This sub-assembly consists of decrete buttons, leaf switches, and a button circuit board. This sub-assembly communicates with the game via the sound button control board. The sound and button control board provides the interface necessary to communicate with the player control and the computer. Communication with the computer is performed over a data bus and an address bus. Both buses are bi-directional, meaning that information can pass in both directions.

The computer and memory board contains the CPU, the memory, the refresh circuitry and teh CRT graphics generator. The CPU is controlled by program information stored with ROM'S (read only memories) and uses the players' controls entering the sound and button control board over the data bus to move the gun left and right, and to fire the gun. All images, including numbers, letters, planes, bombs, ships, and gun are stored in the ROM'S, as well. After the CPU has performed the required operations to the data, new images are stored in

the VRAM (video random access memory) located on the computer and memory board. Another bank of memory is used as "scratch pad" memory and "stack", and is independent from the memory used to store the next frame to be displayed on the TV screen. The sound and button control board is essentially a peripheral device, and as such, it gathers information (a player's button settings) to be processed by the CPU. This board also produces the various sounds required by the system and controls them by configuring a sound generator.

1.4.2 Signal Flow -

There are a number of buses and other significant signal lines which connect the computer and memory board, and the sound and button control board. These lines are first the data bus, which supplies data to and from the CPU board. The address bus supplies addresses generated by the CPU as the refresh circuitry to the external boards. This address bus contains 16 bits which allows full addressing capabilities of the 6800 Microprocessor. The data bus is 8 bits wide. Each bit is represented by a single line, and since this data bus is 8 bits wide, it is sometimes referred to as being a byte wide. In addition to these two buses, there are some special signals on the bus which are referred to as control signals. These control signals are:

(1) Phase 2, which is the basic timing clock for the entire system;

(2) R/W, which is the active high read line for the system;

(3) Reset, which is an active low computer reset line;

(4) VMA, which is a signal which represents Valid Memory addresses as being available on the address bus;

(5) FOAO-3, Which is an active low address decode for addressing

the peripheral interface devices located on the sound and keyboard control board which controls the reading of the buttons .

(6) FOA4-7, which is an active low signal which indicates the decode of the respective addresses required to control the sound generator located at U14 on the sound and button control board;

(7) FOA8-B, Which is an active low signal which indicates the decode of the respective addresses to control sound generator located at U15 on the sound and button control board;

(8) FOAC-F, which is an active low control line indicating the respective address decoder (this signal is used for test only);

(9) IRQ, which is an active low signal indicating interrupt request being made to the CPU. This interrupt request is generated whenever a player pushes any key on the keyboard, or when a coin has been dropped through the chute, or when the new game or next quarter push button have been activated. The CPU is interrupted by this signal, and immediately responds to read the coin switches. Upon completion of the read, the CPU recovers fron the request and continues execution of its' stored program.

1.5 The Computer and Memory Architecture

1.5.1 Introduction-

This discussion of the computer and memory board is intended for orientation of technicians. The areas are covered very lightly, as the main purpose of this manual is understanding how the game works. Block diagram (Figure 5) illustrates

the major circuits found on the computer board. Buses that interconnect these circuits and the direction of signal flow, are illustrated. The major sections in this area are the MPU, the ROMs, the RAMs, the VRAM, and the bus drivers and receivers. The major buses are the address bus, the controls, and the data bus.

1.5.2 Video RAM-

This section generates the master timing signal which is used both to generate a two-phase clock (Ø1 and Ø2) and the horizontal and vertical timing for the video monitor. Figure 6 illustrates the video RAM major operations. The master timing signal is divided down to provide clock sub-multiplies used in both the generation of the sync signals and to read out the contents of the video RAM memory in such a way that information is displayed on the CRT. The sub-multiplies are generated in such a way tht 50% of the time, the CPU can read or write the video RAM while the remaining 50% of the time, the sync and timing signals read out the contents of the video RAM memory.

1.5.3 The RAM Memory-

The RAMs are 4K x 1 bit dynamic devices. The memory in the video RAM is refreshed automatically by reading the information out of memory to the CRT. The stack and scratch pad memory is separately refreshed by a scheme which halts the microprocessor every .2 seconds and then addresses each of the 4K x 1 bit memories. At the completion of each refresh, the microprocessor is allowed to continue form where it was stopped. A total of 12K bytes of RAM are required by the system. All of the memory is addressed by the address bus. The first 4K is stack RAM memory located at addresses OOO-OFFF(hexdeciaml number).

The video RAM memory is located at addressed 8000-90FFF.

1.5.4 I/O Drivers-

The input=output drivers for the CPU have been provided to allow for additional buffing if this board is used in an expanded system. These drivers simply provide power to drive a large number of loads.

1.5.5 Video Generator-

This section is part of the video RAM, and is composed of a shift register and video sync signals which are combined to generate a composite video signal to the monitor. The shift register is loaded with data in byte form, from the video RAM and clocks it in a serial form to the video monitor. Horizontal blanking, horizontal sync and vertical syncs are combined with the serial data, to generate the nominal three-level composite signal used by video monitors.

1.5.6 CPU-

The MPU or CPU is the microprocessing unit. This unit is the M6800 microprocessor. Some of the more important features of this unit that contribute to "ease of use" in the system, are:

(1) Eight-bit parallel processing

(2) Bi-directional data bus.

(3) Sixteen-bit address bus-65K bytes of addressing

(4) 72 instructions-variable length

(5) Seven addressing modes- Direct, Relative, Immediate, Indexed, Extended, Implied, and Accumulator

(6) Interrup vectoring

(7) Two Accumulators

(8) Index Register

(9) Program Counter

(10) Stack Pointer and Variable Length Stack

(11) Condition Code Register (6 codes)

(12) Halt/Go and Single Instruction Execution capability

under parogram control, the CPU processes the data which is provided by both memory and the sound and button control board. The program is stored in ROM memory and it directs the CPU by giving it instructions. Each instruction carries with it, the address where the data is to be found. The program simply steps through the program in a given order. One of the more important points to understand about the 6800 microprocessor is its' start sequence. When the unit is first turned on, or if the reset button is pressed, the microprocessor begins operation at the top of memory. Memory addressed FFFE and FFFF contain the interrupt vector for the reset sub-routine. Thus, anytime the reset signal is activated, the unit will begin its' power-up sequence. In this game, this feature has been taken advantage of by tying a tilt switch on the front door to the reset line. Thus, if someone kicks the unit, the unit will reset and the game will start over. Furthermore, if anyone unplugs the unit from the wall outlet and repeatedly tries to connect and disconnect the unit to get a free game, the unit will power-up into the attract mode. Several manuals have been prepared by microprocessor manufacturers, which explain the CPU and its' operation in great detail. One such manual is the M6800 Microprocessor Application Manual,published by Motorola Semiconductor Products, Inc.

1.6 The Keyboard Interface Architecture

The functions of this interface is to encode the switch closure and interrupt the microprocessor. The computer answers the interrupt after it has completed processing the button data.

1.7 The Sound and Button Controls

One of the main purposes of this board on the game is to interface boards. The other purpose is to control the generation of sound.

1.7.1 The Sound Controls-

The sound is controlled via the microprocessor by treating the sound generator as a peripheral device. The tone is controlled in steps of one-half form full volume to one part out of 128. In addition, there is a noise control, which enables the noise generator, or turns it off. There is also a very low frequency generator set at 10Hz, which is enabled by a separate control. All of the above sounds and tones can be mixed together in any combination. In addition, there is a one-shot control, which allows any of the combinations to provide a pulse of.1 second long. The volume of the sound is controlled by changing the gain of the sound generator, while the tone is controlled by a digital to analog convertor, which in turn, controls the sound generator's voltage controlled oscillator.

1.7.1 The Keyboard Controls

The buttons are interfaced with the microprocessor as peripheral divices. The data coming from the buttons share a bus, and are shared on one peripheral input port.

SECTION II. THEORY OF OPERATION

2.1 The Power Supplies

There are three power supplies in the game. The first is a video monitor power supply, and is detailed in the service manual and parts catalog for either the Wells Gardner Model 22V1001, or the Motorola M-7000.

The second power supply is a 6V unregulated power supply which modifies the power available from the video monitor. Figure 26 illustrates the configuration of this 6V power supply. This unit is used to supply power to the coin counter, which is located on the front coin door of the unit.

This power supply rectifies the filament voltages in the monitor with a full wave bridge and provides an 8.5V DC level to be used by the coin counter. The +8.5V is available between pins 6 and 3 of P1 on the video monitor connector.

The third power supply supplies regulated voltages. These regulated voltages are +5, -5, +12 and -12. Detailed descriptions of this power supply are available in the Parts and Service Manual for the Calex Model MPS-OF-45.

2.2 Operation of the Game's Digital Circuitry

The digital circuitry of the game is composed of basically three printed circuit boards. The first is the computer board, and the following figures and discussion relay how that board operates. Figure 7 (Sheet 1 of 1C30013), illustrates the address decoding associated with the game. There are basically 20 special addresses used in the game. These special addresses are located at F048 to

F04B, and from F0A0 to F0AF. The address lines A00 through A15 are combined through appropriate ands and nands to provide the decodes for these addresses. Each of these addresses perform a special function. For example, F04A automatically clears the TV. F04B clears the time registers.

Figure 7 also illustrates the operation circuitry required to generate the two clocks for the microprocessor from a single clock source.

Figure 8 illustrates the CRT select and automatic clear functions. The CRT select is based upon the detection of any address in the range of the video RAM. When this occurs at the proper phase of the microprocessor clock, then the CRT is selected, and all addresses directed to the CRT are channelled to the video RAM.

The automatic clearer of the monitor is started when a write at the address, F04A, is generated. This address then sets a flip-off, which waits until the top of the picture occurs, and then writes all zeros into the video RAM memory, by generating the signals WE and CLEAR WRITE. When the top of the picture occurs again, these signals are removed. Thus, in one complete scan from the top of video RAM to the bottom, the memory has been written with zeros. This effectively clears the images on the monitor.

Figure 9 illustrates the computer and memory interfaces. The computer is an 16800, which is interfaced to the data lines through a set of receiver and transmitter devices. When valid memory address (VMA) and read write (R/W) both occur, the receivers are

enabled, and the microprocessor examines the data supplied. In all other cases, the transmitters are enabled, and the data lines are following the states provided by the microprocessor.

The address lines provided by the microprocessor are buffered through a set of tri-state buffers. Address lines A0 through A5 are controlled by the bus available signal (BA). When bus available is active, the address lines A0 through A5 are put in the tri-state mode. This allows these address lines to be driven by the refresh circuitry described later. Address lines A0 through A15 are controlled by the buffered bus available line (BA). When the bus available buffer is active, then the high address bits are set in the tri-state mode.

Three additional signals are supplied to the microprocessor for special controls. The first is power-up reset, which allows the microprocessor to start the game when the unit is plugged in. The second is an interrupt request (IRQ), which is used to detect the occurrence of data coming from the keyboards. The read signal is the halt line (HLT). This signal is used by the refresh circuitry to halt the microprocessor. When the microprocessor is halted, the bus available signal becomes active, and the low address bits are tri-stated, so that the refresh circuitry can refresh the random access memories used for temporary storage.

Figure 10 illustrates the circuitry which supports an internal timer and the refresh circuitry. The internal timer uses a 500 Hz clock, which is counted down to 16 Hz. This 16 Hz signal is then supplied

to two 4-bit counters, which can keep track of time between 1/16th second and 16 seconds. By reading these counters at address F04B, the data is supplied to the microprocessor which represents time. In order to clear the timer, any write of data to address F04B, clears the counter back to zero seconds.

This timer is also a deadman timer which resets the microprocessor if it ever times out.

The refresh circuitry has a basic clock of 500 Hz. This clock is labelled CKRF. Whenever this signal becomes active, the refresh is enabled, and on the next phase one, the halt signal is generated. When the microprocessor responds by making bus available active, a synchronous counter generates all of the addresses between zero and 3F on each phase of the microprocessor clock. When the address 40 is generated, the refresh cycle is ended and the refresh clock is reset.

Figure 11 illustrates the horizontal timing of the video monitor. The video horizontal timing is generated from a 5.185 MHz crystal oscillator. This oscillator generates the basic clock for the game. Eight phases of this clock constitute the timing required by one byte. On the sixth phase of the clock, the signal LOAD is generated. During phases 5 and 6, buffered phase 2 is generated (BØ). During phases 4, 5, 6 and 7, the phase source signal is generated ($Ø_1$-SOURCE). During phases 2 and 3, the phase 2 sync signal is generated ($Ø_2$-SYN). The Load signal is used to read the video RAM memories. The buffered phase signal is used during the read portion of the video RAM associated with the monitor scan and the phase 2 sync signal is used during the microprocessor read or writing of the video RAM.

The 5.185 MHz clock is counted by two synchronous counters to generate the horizontal timing. On completion of a full count, a flip-flop is toggled between two states. The first state (HD) is used to count the horizontal retrace time. This is set to be equivalent to 8-byte time periods. The other state is $\overline{\text{HD}}$. During this state, the counters count the number of bytes displayed on the video monitor. This time has been set to 32 bytes long. In order to generate the proper horizontal sync, special logic has been set up to detect the end of the state associated with HD. Thus, the horizontal sync (HDR-SYN), is generated during the last 5 bytes of the horizontal retrace time.

The horizontal addresses for the video RAM are multiplexed by 2-1 multiplexes. These multiplexes are controlled by the CRT enable signal ($\overline{\text{CRT}}$). When the CRT enable is active, the multiplexer allows the addresses from the microprocessor to access the video RAM. When this signal is not active, the horizontal timing generates the addresses for the video RAM.

Jumpers have been provided for selection of various signals to support many different dynamic RAMs. Table II gives a listing of the RAM type and the jumpers provided on the board. This table shows the configuration for each jumper required to support that type of RAM. In addition to these jumpers, there is also a jumper select on the horizontal sync, which allows a little more delay on the left edge of the picture tube, before the scan starts. This jumper is located on the board between E13 and E14, and is labelled W5 on the drawings.

The line counter is illustrated in **figure** 12. This counter basically counts each line to be supplied to the video monitor. There is a total of 256 such lines on one vertical scan of the monitor. Every horizontal scan of the monitor is counted in two synchronous line counters. The outputs of these synchronous line counters give the address for a horizontal line. The line counter counts in three separate modes. The first is the vertical retrace count. When the last line is put out at the bottom of the monitor, the line counter provides a vertical sync pulse, which has its width set to 31 lines. The second mode counts 4 blank lines at the top of the picture tube, and the third mode is to count the 256 lines across the face of the monitor.

Basically, the unit works as follows: The signal VD is the vertical downtime, or the vertical retrace. When this signal is active, the counter starts at a preset value, which allows 31 counts until the carryout is generated. When the carryout is generated, the vertical downscreen signal is toggled, and the counter starts at zero with a preset value of zero. Since this occurs at the top of the picture, a flip-flop remembers this state, and when the counter reaches its first count of 3, the flip-flop is cleared, and the counters are cleared back to zero. Then the third mode begins, with the counters counting 256 lines, until another carryout is generated, which starts the process over again.

The CRT control signal ($\overline{\text{CRT}}$) controls two multiplexers which select

the outputs from the line counter or the addresses available from the microprocessor. Figure 13 illustrates the video output circuitry. The data read from the memory is loaded into an output shift register, and this data is shifted one bit at a time, to generate the data visible on the TV monitor. These dots are then combined with blanking signals, which turn the monitor off during the horizontal retrace and the vertical retrace. The signal is then combined with the horizontal sync and the vertical sync to generate a composite video which is supplied to the monitor. The composite video is a three-level signal, ground being synchronization voltages, the middle state being the off condition of the dot, and the third level being the on condition of the dot. Also illustrated on this figure is the video RAM selects required for the dynamic RAMs. As can be observed, these selects are basically associated with the control signal ($\overline{CSJ}$). This control signal alternately selects one line of data from each of the two banks in memory.

Figures 14, 15 and 16 illustrate the memory organization of the game. Bank zero is 4K of random access memory dedicated for temporary storage and stack operations. Bank 8 is one-half of a video RAM, and is located at addresses 8000 to 8FFF. Bank 9 is the other half of the video memory, which is located at addresses 9000 to 9FFF.

Then Figure 17 illustrates the interfacing between the video RAM data bus and the microprocessor data bus. Microprocessor data bus is a bi-directional data bus, and it is controlled by the signal RE. When RE is enabled, data from the video RAM is made available to the micro-

processor data bus. Data from the microprocessor data bus is always available to the video RAM, and is stored into the video RAM by strobing the write line. There is one exception to this when the automatic clearer is generated, the write enable signal (WE) is active, and it forces all of the data lines coming form the microprocessor to be at logical state zero, thus effectively writing all zeros into the video RAM. Figures 18, 19 and 20 illustrate the organization of the game ROMs. Each of these ROMs is a 16K bit memory. Each is organized into 2K 8 bit bytes. Address 11 (ALL) selects which of two ROMs supplies data for address decodes associated with a 4K bank. Thus, the decode signals CM1 and CM2 select read only memory in the 1000 to 1FFF, or 2000 to 2FFF, respectively; likewise, CM3, CM4, and CM5 address 4K banks of ROM memory. The board has been organized with jumpers so that the 16K bit ROMS may be replaced withe 32K bit ROMs for future expansion and parts availability. One additional read only memory exists in the system,It is amemory with 2K bytes located at the top of memory. This device is usually in most games, an EPROM. The final figure which illustrates the operation of the computer and memory card, is Figure 21. This figure illustrates the address decoding necessary, together with the bank select controls for each of the computer memories available in the unit. Each address decode is combined with valid memory address, and then the computer select commands signals CM0 through CM9 are generated. Also illustrated in this figure is the data buffering required between the scratch pad dynamic

memory and the microprocessor data bus. Whenever a read of the scratch pad memory is made, the data from the scratch pad memory is buffed onto the active high data bus. The above discussion completes the description of the computer and memory printed circuit board contained within the game.

2.2.1 Button and Sound Interface Digital Logic-

The button and sound interface digital logic is rather simple. This board basically consists of three peripheral interface adaptors. The first interface adaptor is assigned to the individual button switches. The second and third PIAs are associated with controlling two sound generators. The button PIA is located at addresses F0A0 through F0A3, and is illustrated in Figure 22. Data from the microprocessor is supplied to registers located in the PIA at these addresses. This data is used to read the button Figure 23 illustrates the control of one complex sound generator through the utilization of a PIA. This PIA is located at addresses F0A8 through F0AB. Port A of the PIA controls the tone of the sound generator by providing a digital data word to a D to A converter which controls the sound generator's voltage controlled oscillator. This voltage which controls the VCO, varies between zero and -5V. The other port PB controls the complex sound generator's mixer envelope and amplitude. The upper 3 bits of this port allow the section of one of eight amplitudes fo the sound output. Each of these amplitudes is one-half of the previous sound amplitude. This is the volume for control from 1, 1/2, 1/4 through 1/64, 0. The magnitude of the output

of the complex sound generator is controlled by variable potientiometer. This signal is than amplified and supplied to the external speakers. A similar circuit is illustrated in Figure 24, which controls the volume and the sound on the separate sound channel. One other function is performed on the button and sound control board. This deals with providing pulses to operate the coin counter. The coin counter utilizes the first PIA located at FOA2, port B, bit 5 to provide one pulse to the coin counter. When this signal is enabled, the output transistor is turned on and power is supplied to the coil of the coin counter relay. This signal is disabled after a period of 60 milliseconds and the coin counter relay is relaxed.

2.2.2 <u>The Button Interface Digital Circuitry-</u>

There is the button input board on the unit. The schematic for this keyboard is shown in Figure 25. When any of the buttons are depressed, the schmitt trigger, which is illustrated in Figure 25, detects the contact closure, debounces the switch and provides a data encode that represents the button associated with that switch closure. This data is then available for the input PIA located at address FØAØ. To prevent the microprocessor from overlooking any of the data whenever a data available signal is generated by the keyboard encoder, an interrupt request is supplied to the PIAs located on the keyboard interface and sound control board. This interrupt must be removed by the microprocessor when it reads the data available on the keyboard encoder.

SECTION III. AC POWER AND SPECIAL CABLES

3.1 INTRODUCTION

This Section is to describe all the other wiring in the game.

3.2 AC WIRING

The AC Wiring is Illustrated in Figure 27. The AC input is first Illustrated by a High Voltage Over-Voltage Protector and then a Line Filter and Fuse. The Filtered AC is then distributed to the Lights, TV Monitor and the DC Power Supply.

3.3 COIN COUNTER AND RESET CABLE

Figure 28 Illustrates the Re-Set and Coin Counter Cable. This Cable takes the + 6 Volts on the monitor to the Sound Board, where it is switches to control the coin counter. On the same connector at the sound board, is the reset signal which is routed to the coin door, to allow the reset of the game.

3.4 OTHER CABLES

The other Cables in the game Include the following;

(1) The Keyboard Cables; which connect the sound board to the Keyboard Interface board.

(2) The Coin Slot Cable; which is connected to the left keyboard (looking at the front of the cabinet);

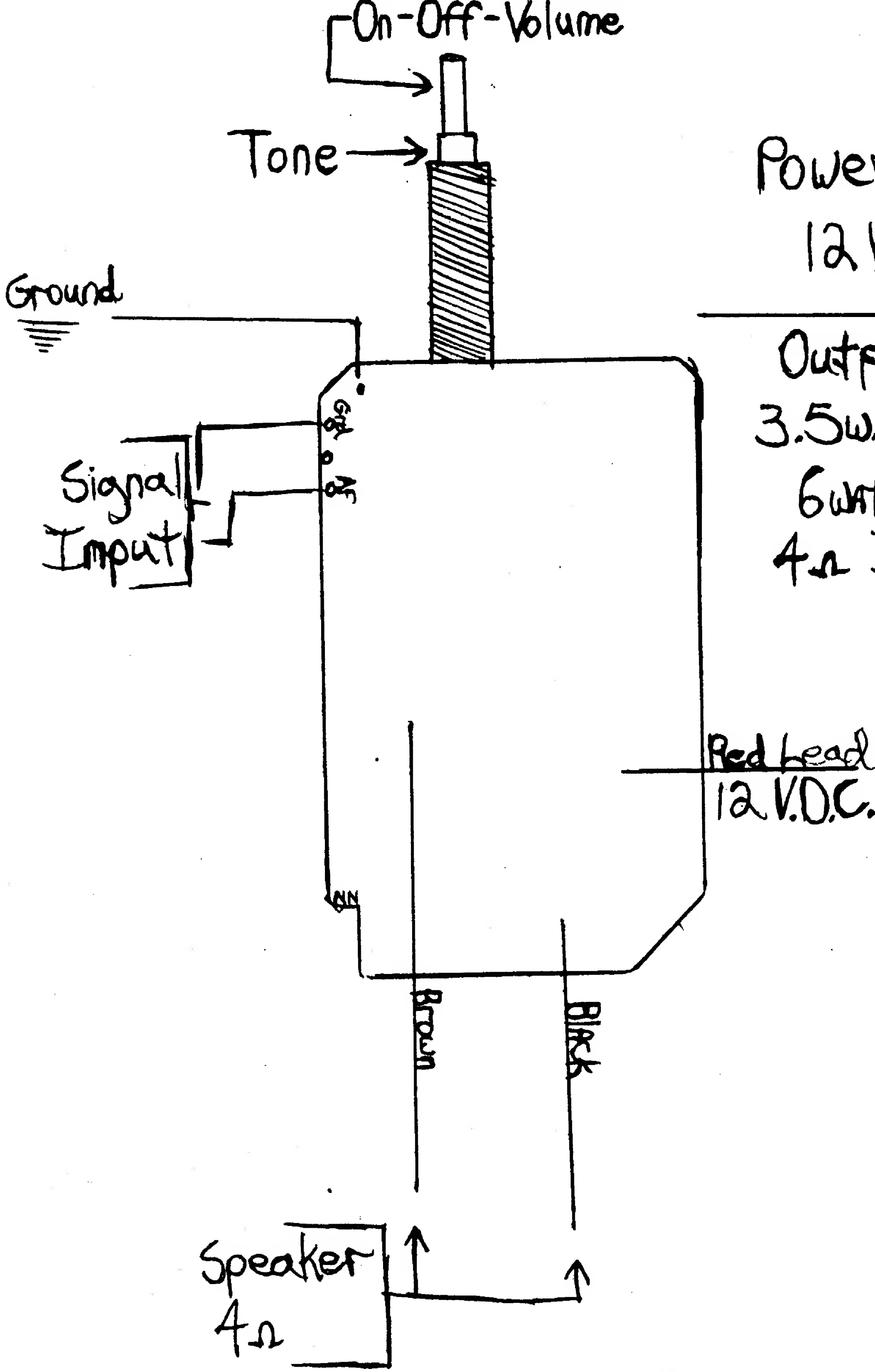
(3) The Game Start Switches; which are connected to the right keyboard (looking at the front of the cabinet);

(4) Audio Amplifier Cables, which connect Audio Amplifier to the Speakers and the Sound Board.

All of these cables and their parts list can be found in the attached parts list of running list.

3.5

6w. Mono Amplifier



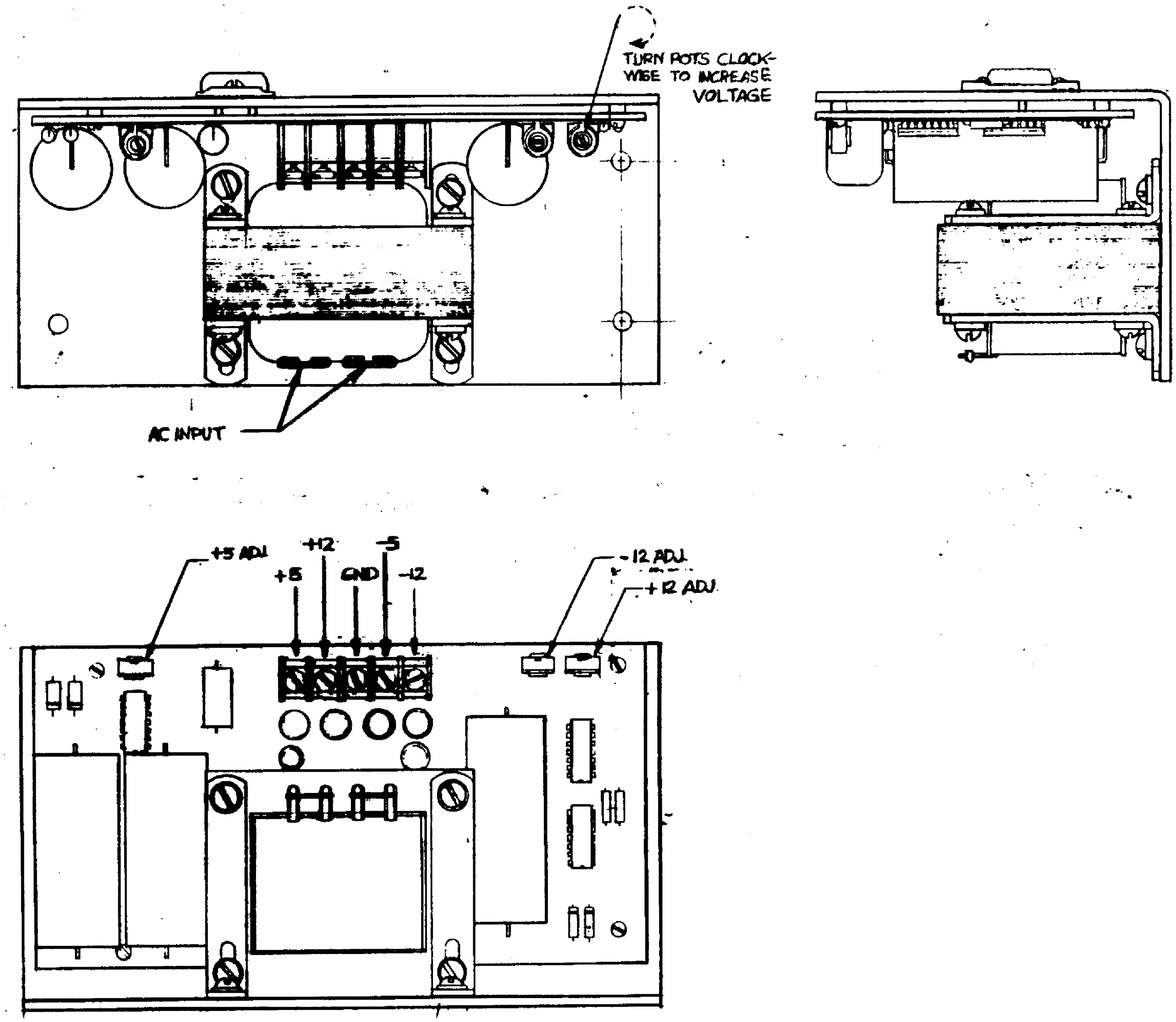
Power Supply
12 V.D.C.

Output
3.5w. RMS
6 watts Peak
4Ω Impedance

TABLE II

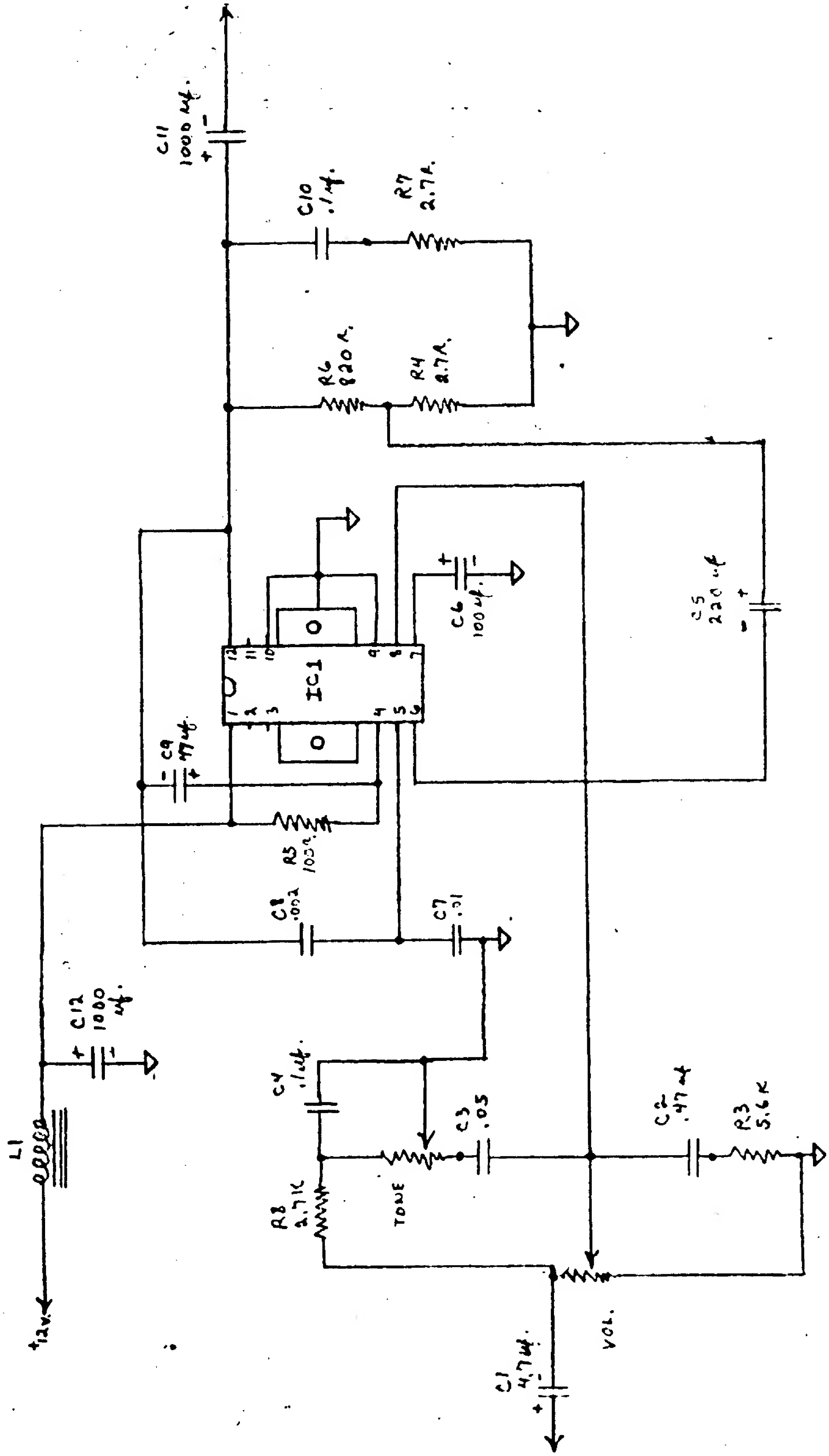
Jumper Configurations

RAMS \ JUMPERS	CEO	CE1	CE	WRITE	W/R	
TMS 4060	E1-E2	E4-E5	E7-E8	E10-E12	E25-E27	
MM 5280	E1-E2	E4-E5	E7-E8	E10-E12	E25-E27	
SMI 4200	E1-E3	E4-E6	E7-E9	E10-E11	E25-E26	
2107	E1-E2	E4-E5	E7-E8	E10-E12	E25-E26	
ROM	$\overline{\text{All}}$	$\overline{\text{6XXX}}$	$\overline{\text{7XXX}}$	NOTES		
2316	E22-E23	E16-E17	E19-E20	USE ALL SLOTS		
2317	E24-E23	E17-E18	E20-E21	REMOVE U10, U9 AND U[illegible]		



CABINET POWER SUPPLY PSI

FIGURE 1


C11
1000 uf.
C10
.1uf.
R7
2.7Ω
R6
820Ω
R4
2.7Ω
C6
100uf.
C5
220 uf
IC1
C9
47uf
R5
100Ω
C8
.002
C7
.01
C12
1000
uf.
L1
+12v.
C4
.1uf.
C3
.05
TONE
R8
2.7K
C2
.47uf
R3
5.6K
VOL.
C1
4.7uf.

IC1= TBA-810 S

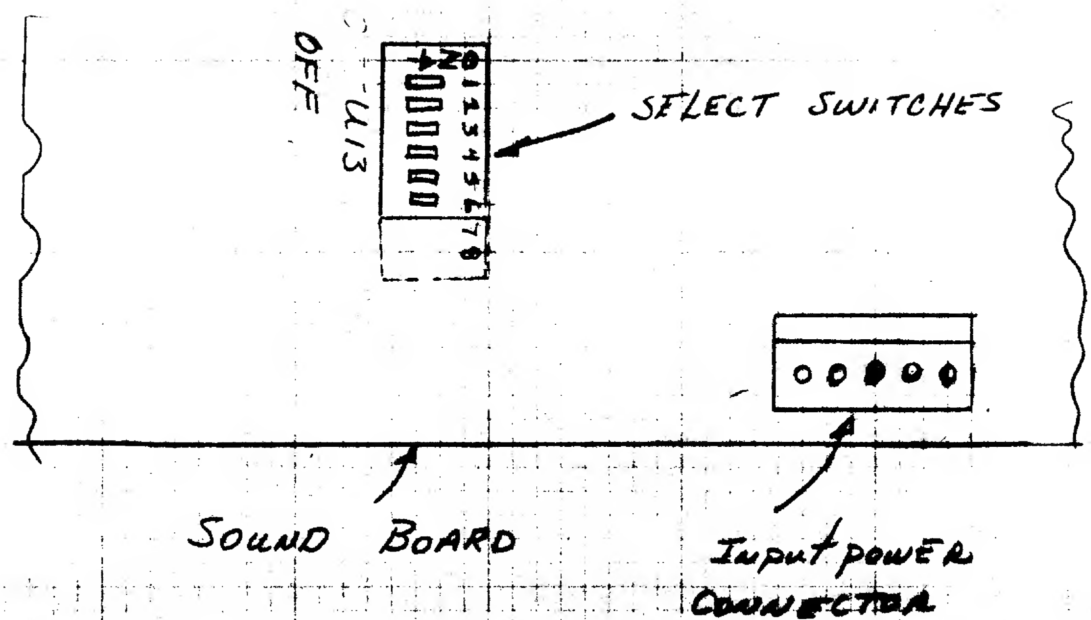


FIGURE 2 - SELECTION SWITCHS

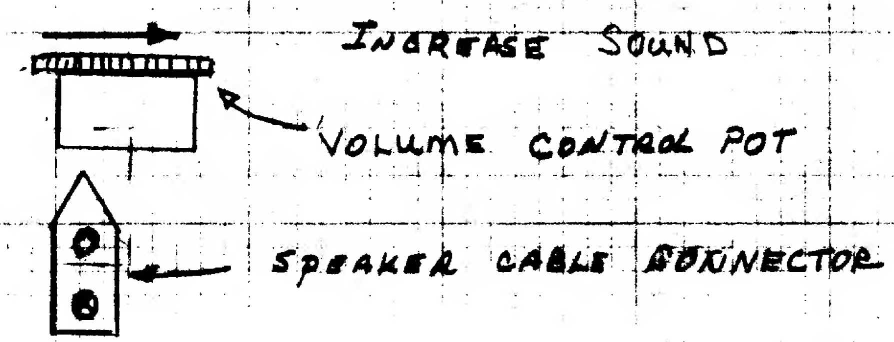


FIGURE 3 - VOLUME ADJUSTMENT

SWITCHBANK U13 (SOUND BOARD) ADJUSTMENTS

(SEE FIGURE 2, PAGE 28)

The switchbank is divided into 3 sections: (1) Coin Mech.#1 (2) Coin Mech. #2 and (3) Gun Count
Coin Mech. #1 and Coin Mech. #2 have switches and gun count has 1 switch.

Coin Mech. #1= Sw. #1 & Sw. #2
Coin Mech. #2= Sw. #3 & Sw. #4
Gun Count= Sw. #6

Coin Mech. (#1 or #2) CONFIGURATION:

SWITCH	SETTING	PRICE		
Sw. #1 (3)	Sw. #2 (4)	CREDIT		COIN
OFF	OFF	1	(25¢)	1
ON	OFF	1	(50¢)	2
OFF	ON	3	($1.00)	1
ON	ON	5	($1.00)	1

Maximum credits allowed on game is 15.

Gun Count Configuration:

Sw. #6	# of Guns
OFF	3
ON	4

Important: During game assembly all switches are set to "OFF" position (1 credit for 25¢ & 3 guns)
Maximum score that can be obtained is 50,000 after which score will revert back to 0000.

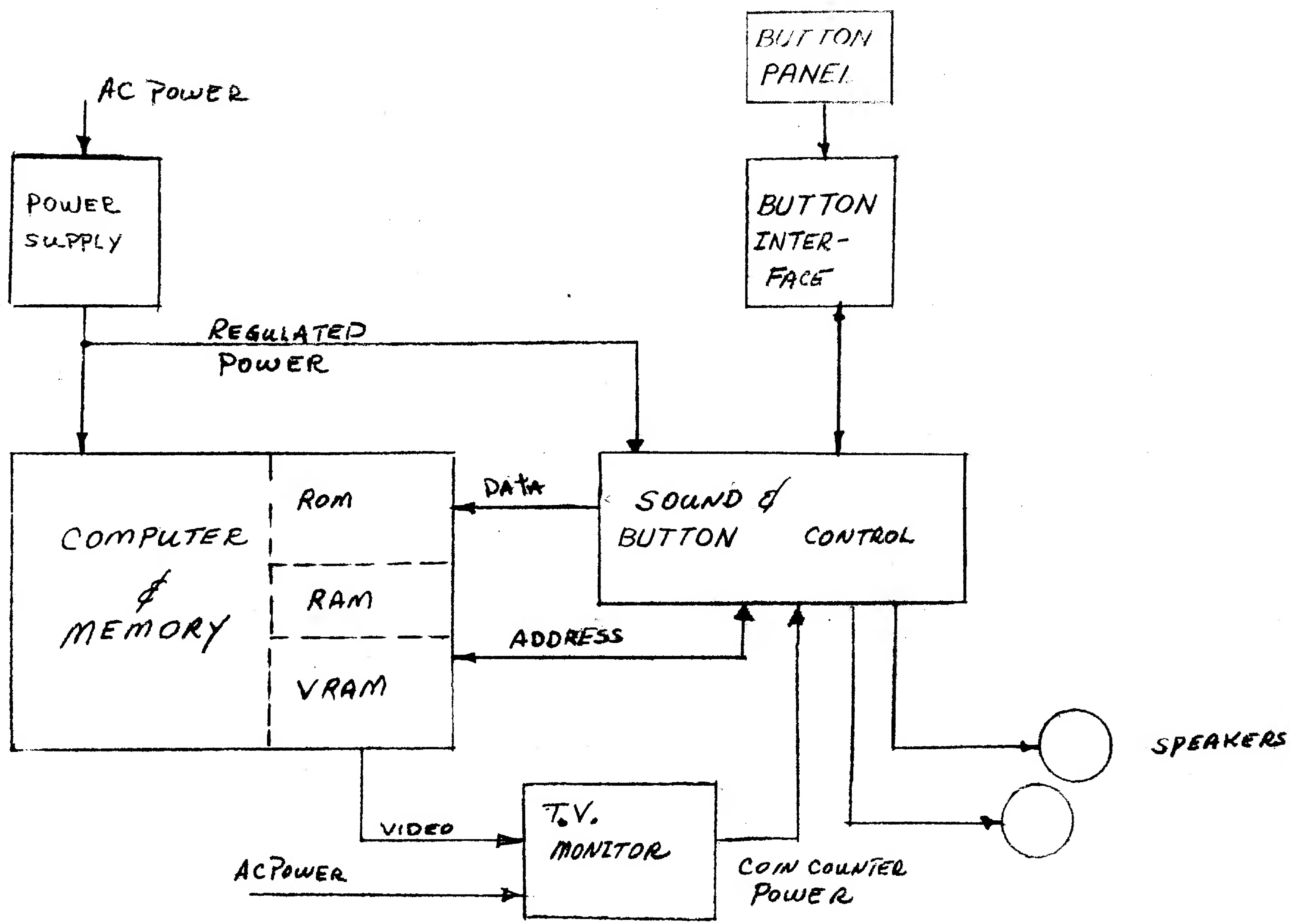


FIGURE 4 SYSTEM BLOCK DIAGRAM

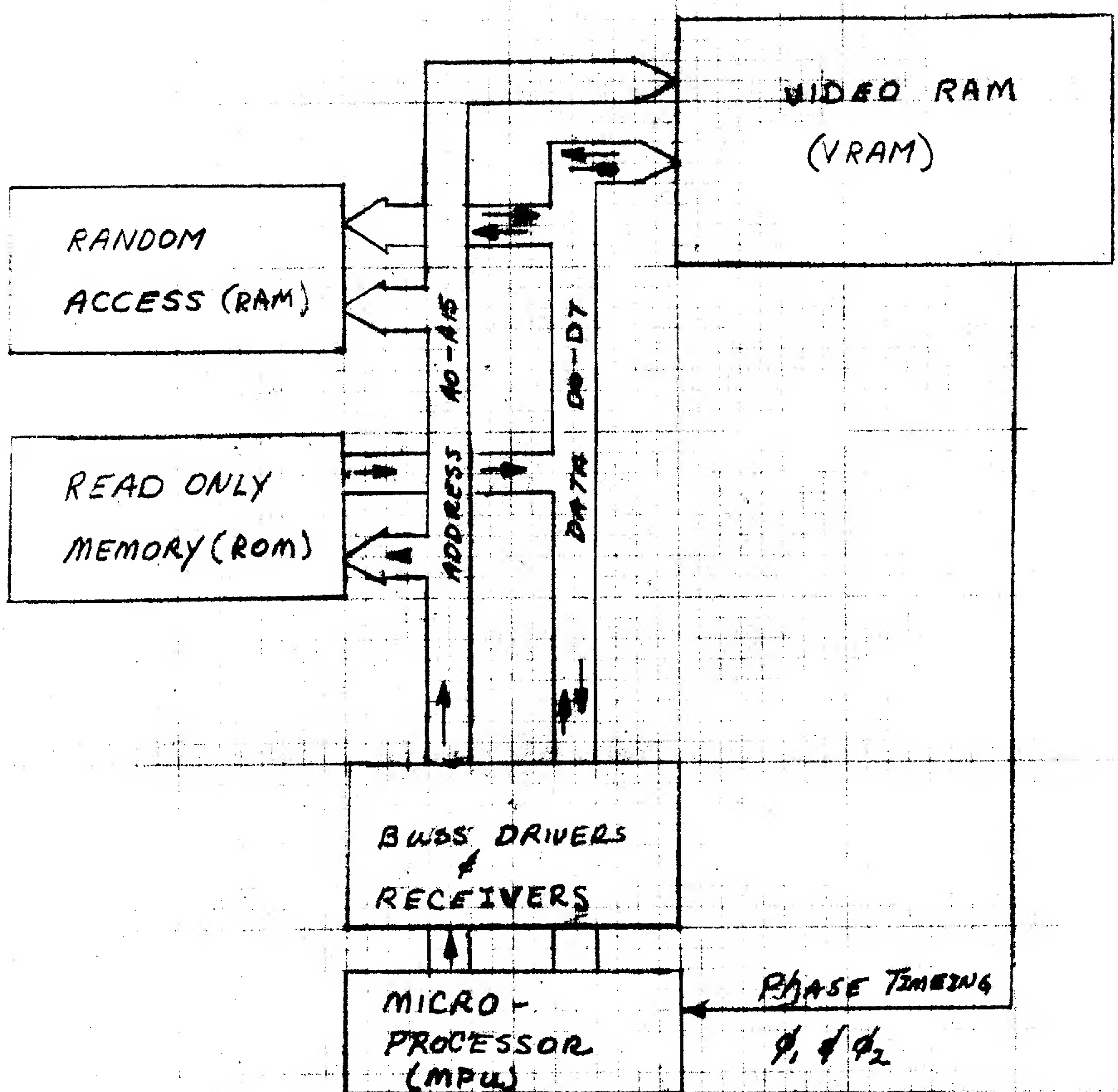


FIGURE 5 COMPUTER AND MEMORY BOARD

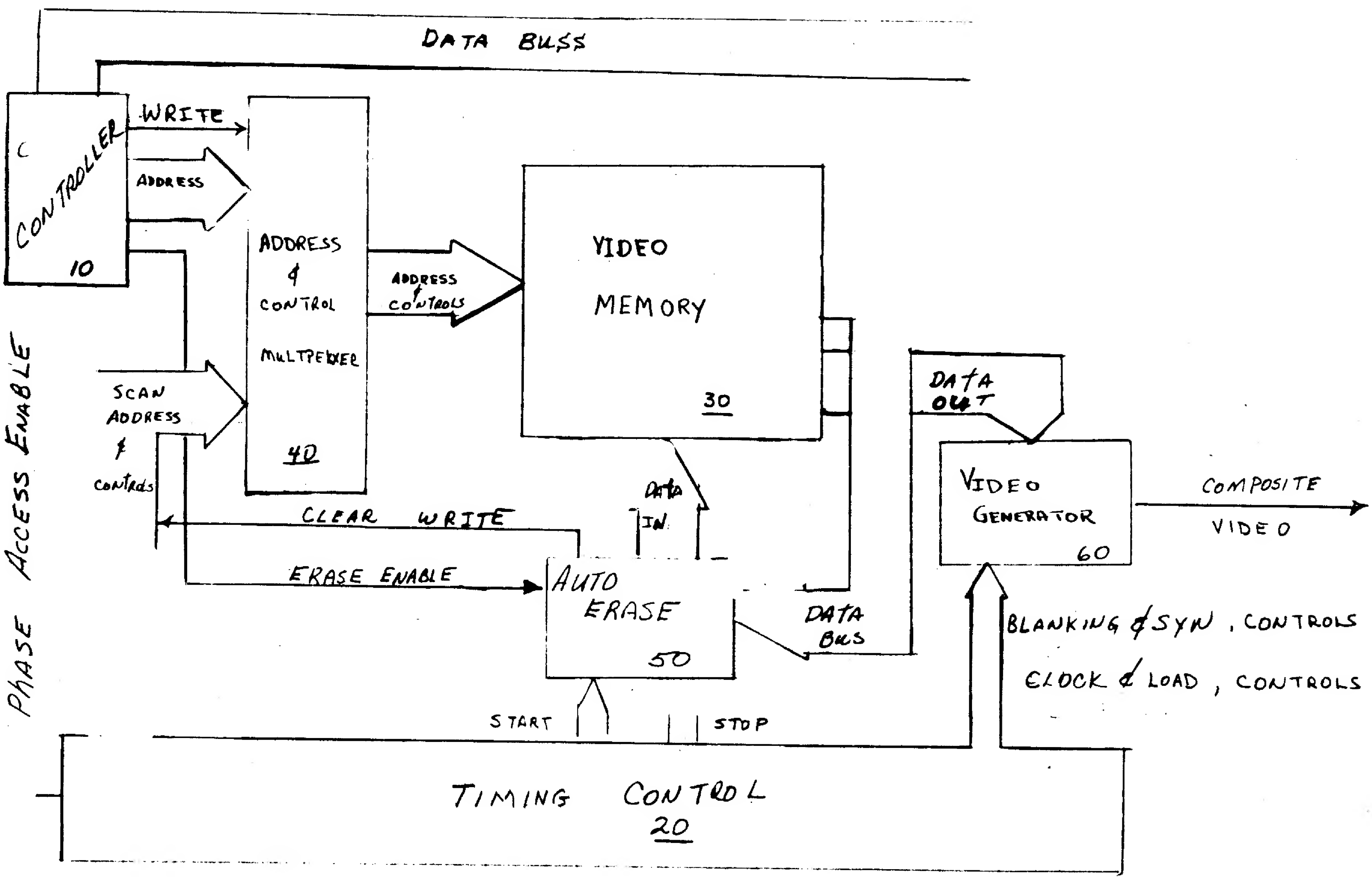
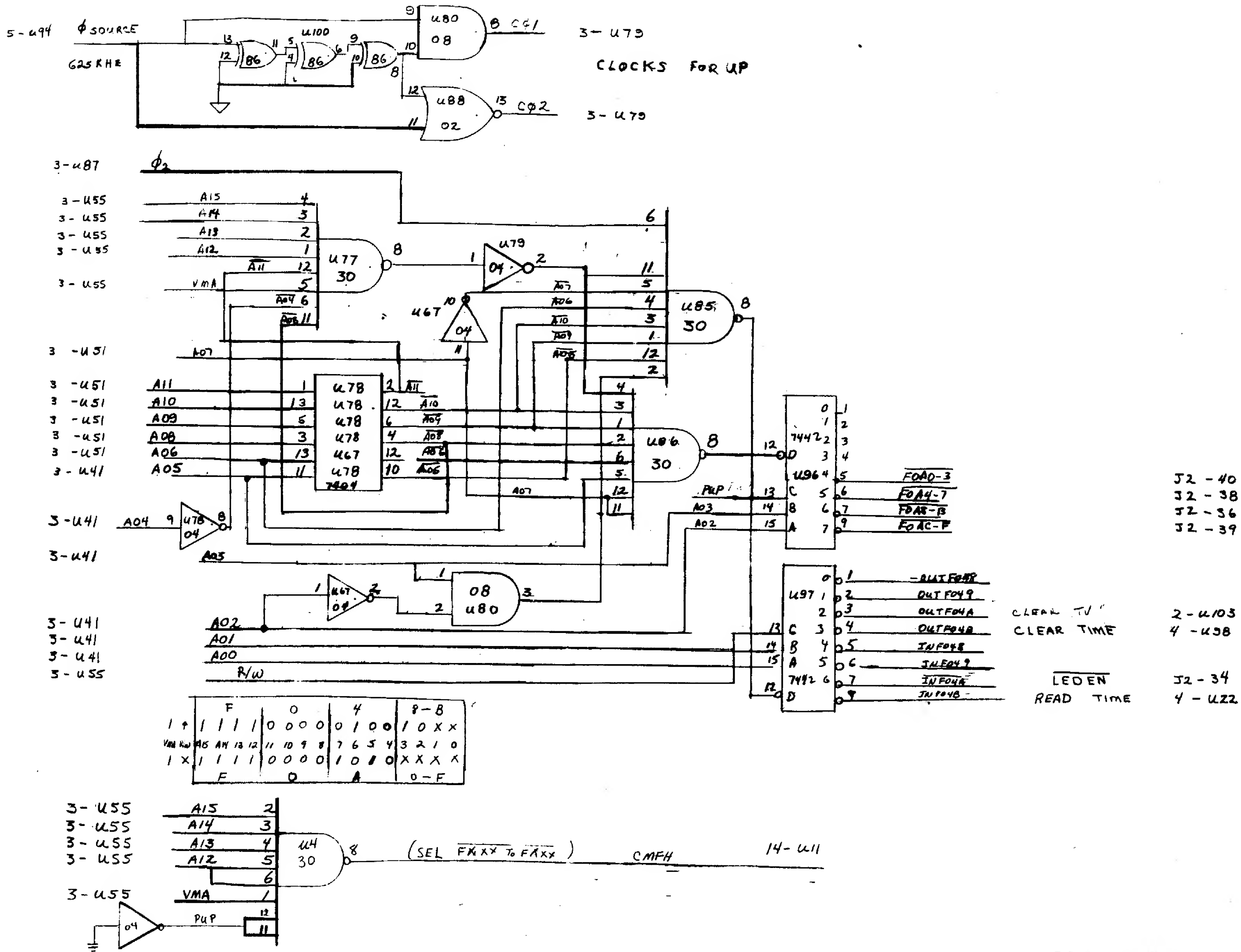


FIGURE 6 VIDEO RAM



ADDRESS DECODES

Computer & Memory PCB

FIGURE 7

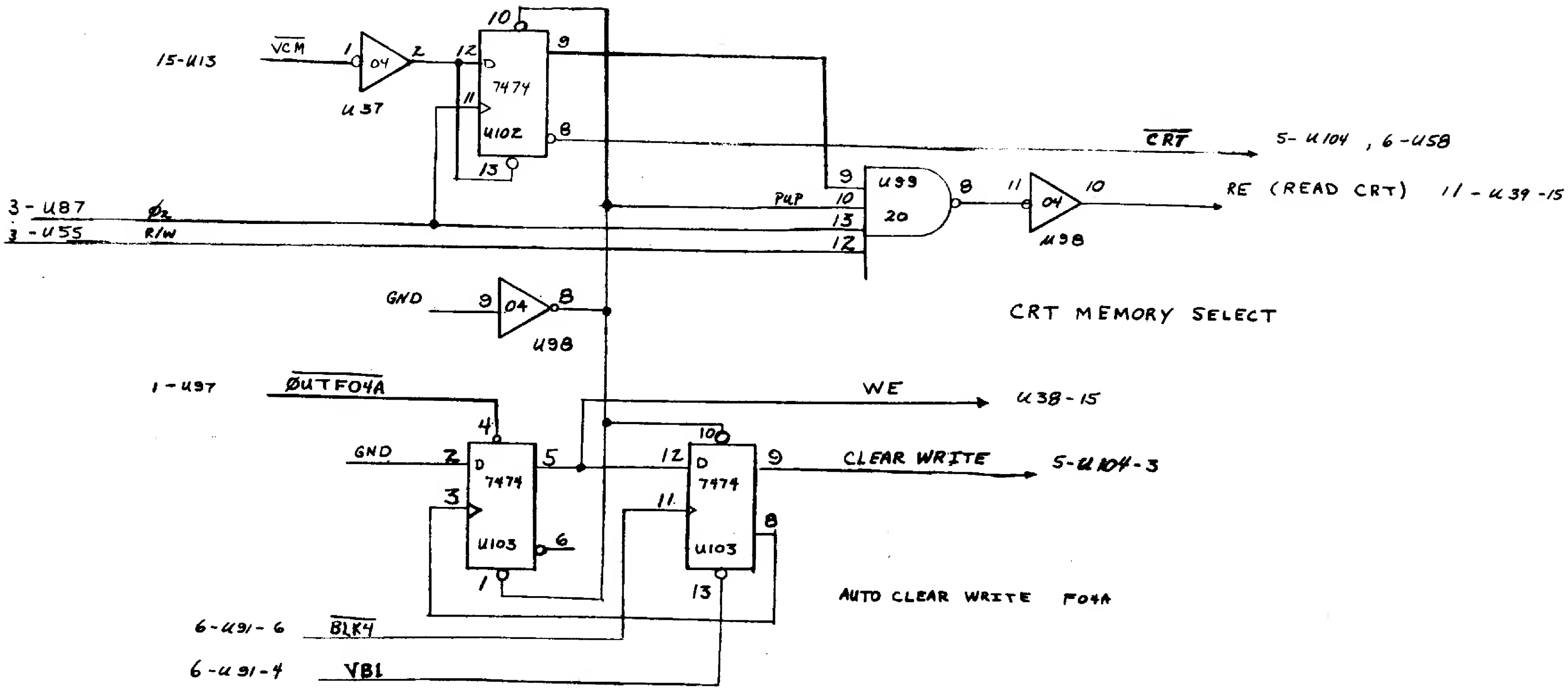


FIGURE 8

CRT SELECT & AUTO CLEAR
Computer & memory PCB

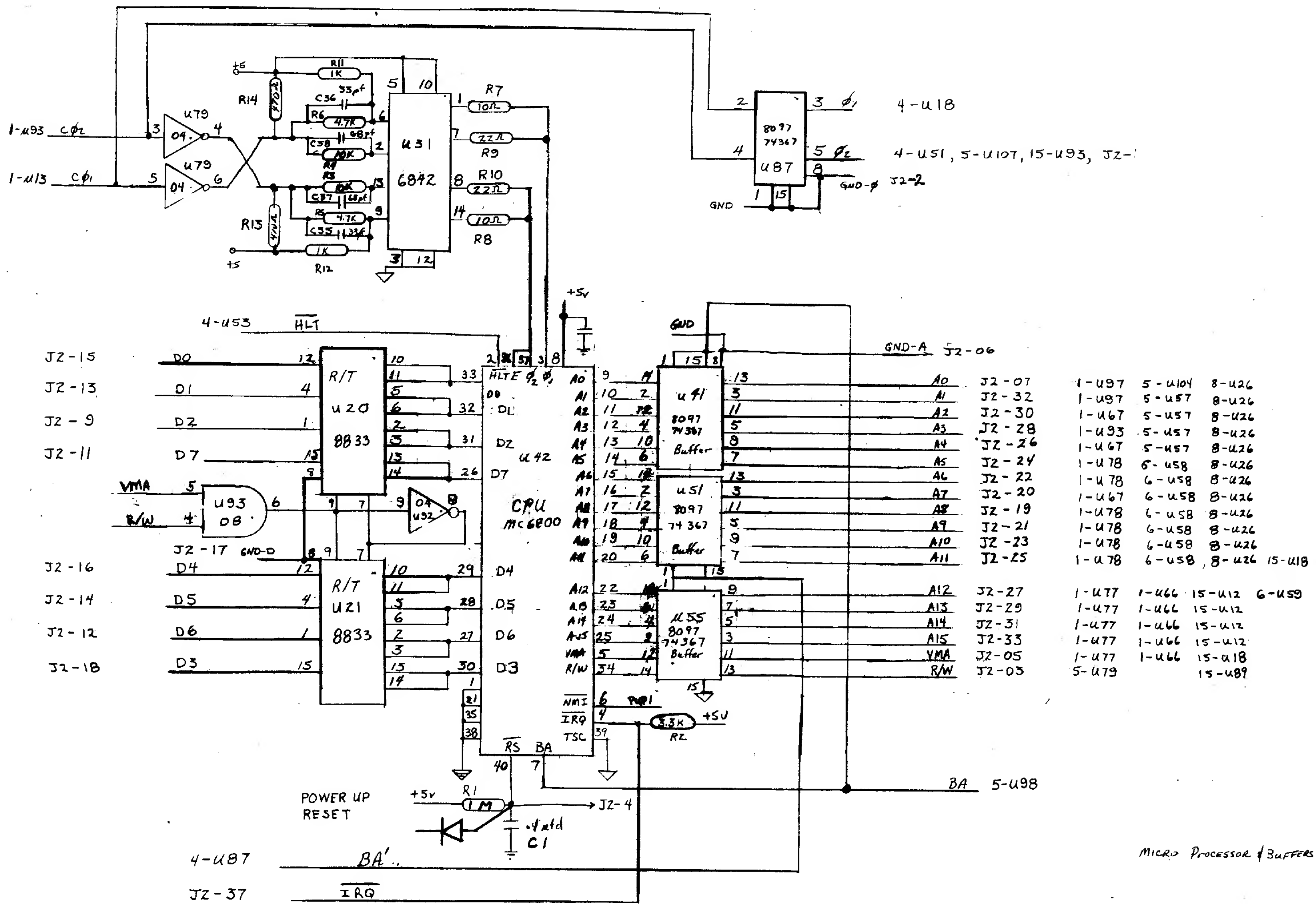


FIGURE 9

Computer & memory PCB; Clock and CPU

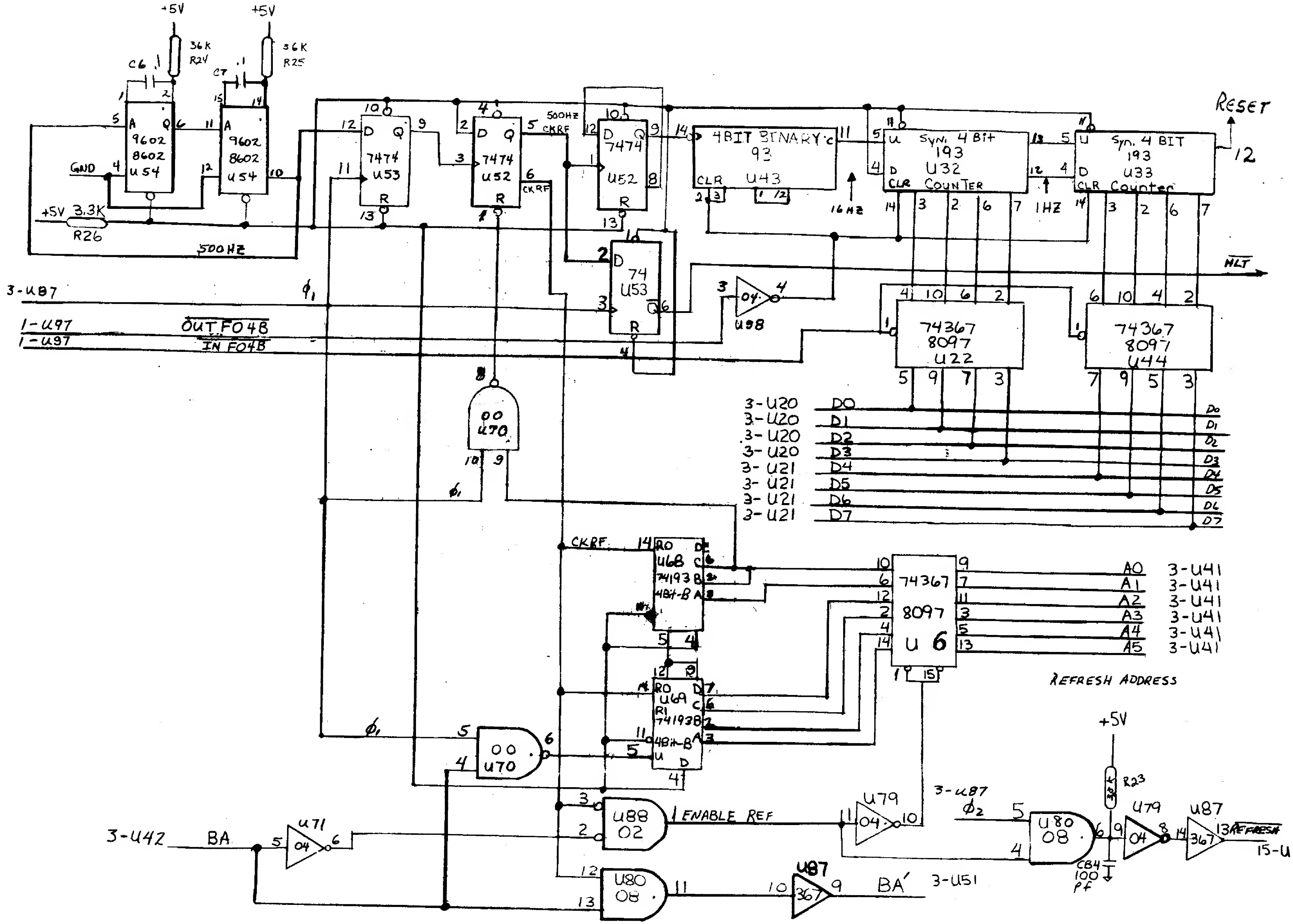
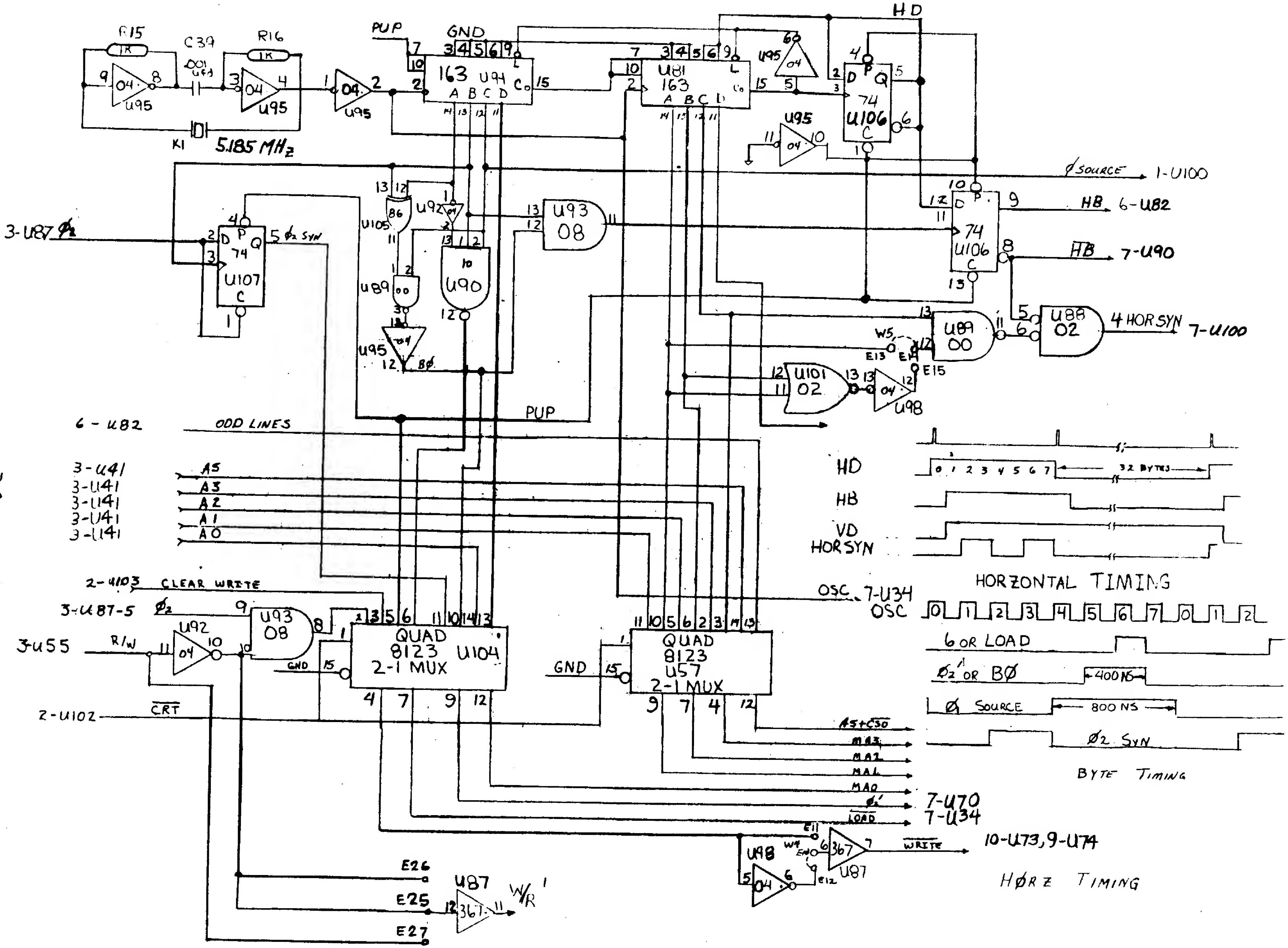


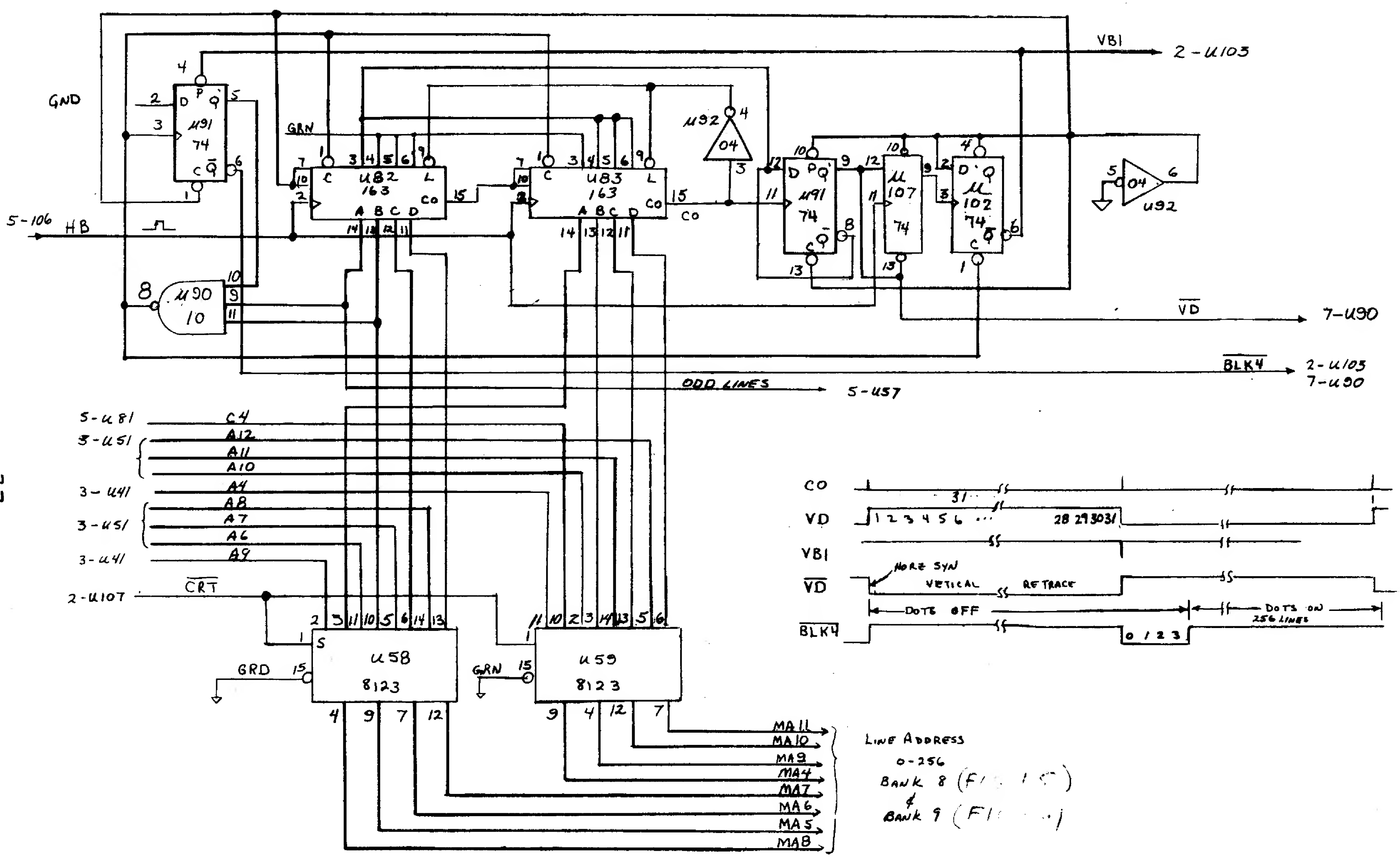
FIGURE 10

Computer & Memory PCB, Time & Refresh



R15
C39
R16
1K
.001
04
U95
K1
5.185 MHz
PUP
GND
163
U94
U81
U106
74
U107
HD
U93
08
U90
U89
00
U105
86
U92
U101
02
U88
4 HORSYN
7-U100
ø SOURCE
1-U100
HB
6-U82
7-U90
3-U87 ø2
5 ø2 SYN
U98
W5
E13
E14
E15
6-U82
ODD LINES
3-U41
A5
A3
A2
A1
A0
2-U103
CLEAR WRITE
3-U87-5
ø2
3-U55
R/W
2-U102
CRT
QUAD
8123
2-1 MUX
U104
U57
OSC
7-U34
HD
HB
VD
HORSYN
32 BYTES
HORZONTAL TIMING
6 OR LOAD
ø2' OR BØ
400 NS
ø SOURCE
800 NS
ø2 SYN
BYTE TIMING
A5+CS0
MA3
MA2
MA1
MA0
ø2'
LOAD
7-U70
7-U34
E11
W4
E10
E12
367
U87
WRITE
10-U73, 9-U74
HØRZ TIMING
E26
E25
E27
W/R'

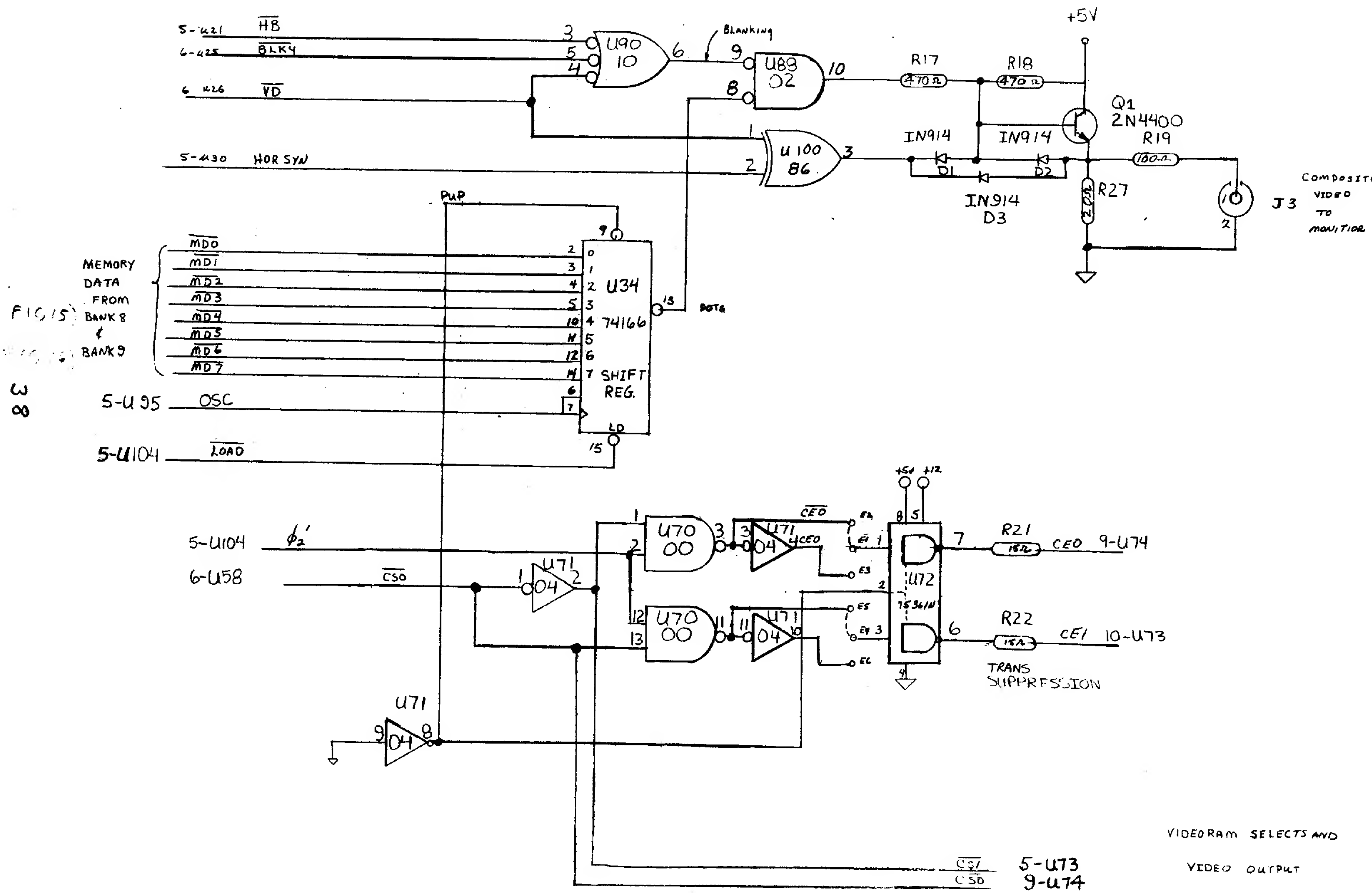
FIGURE 11



u25 - 24-11
u22 10 21

FIGURE 12

LINE COUNTER



VIDEORAM SELECTS AND VIDEO OUTPUT

FIGURE 13

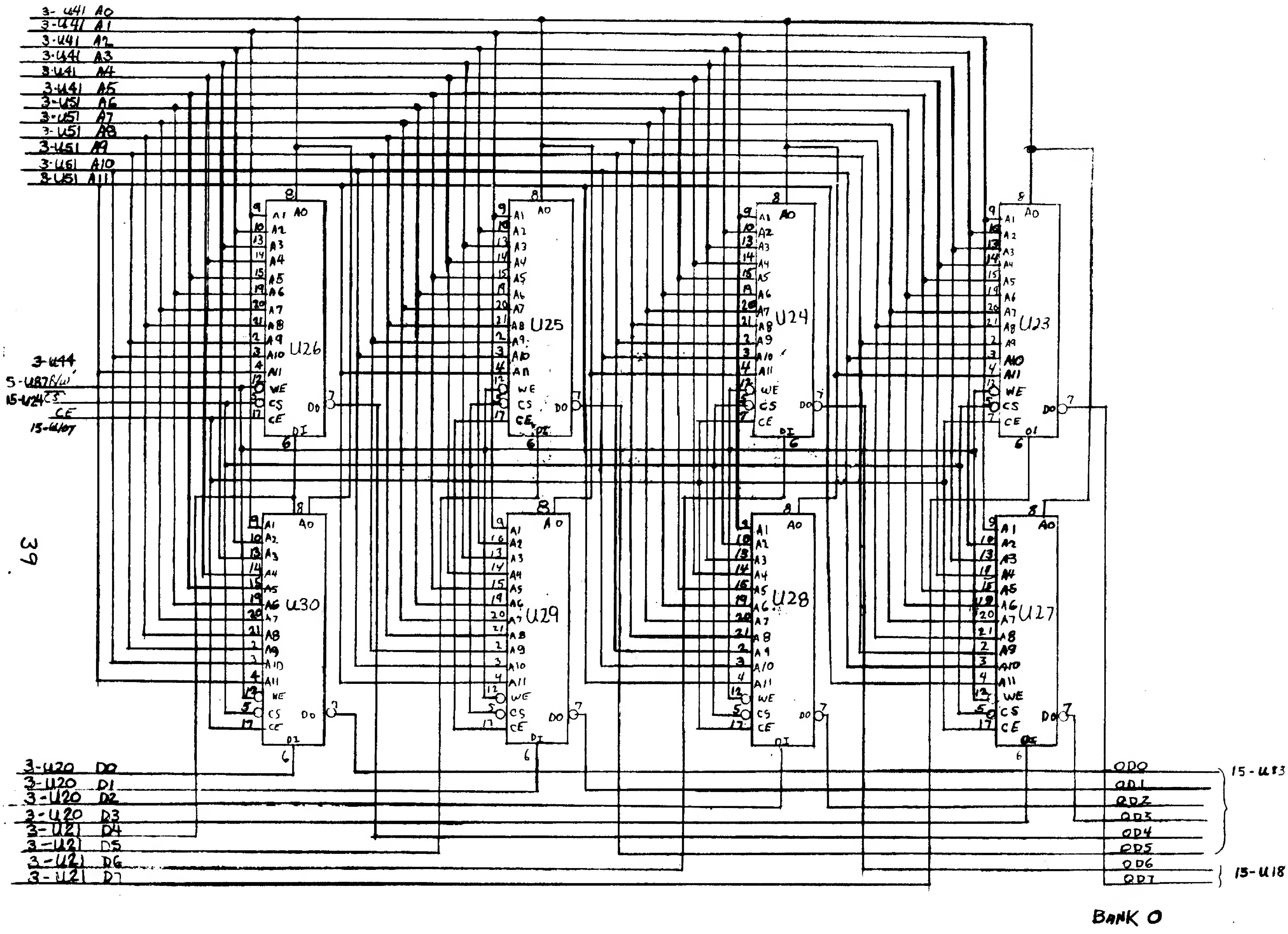

3-U41 A0
3-U41 A1
3-U41 A2
3-U41 A3
3-U41 A4
3-U41 A5
3-U51 A6
3-U51 A7
3-U51 A8
3-U51 A9
3-U61 A10
3-U51 A11
3-U44
5-U87 R/W
15-U24 CS
CE
15-U107
U26
U25
U24
U23
U30
U29
U28
U27
3-U20 D0
3-U20 D1
3-U20 D2
3-U20 D3
3-U21 D4
3-U21 D5
3-U21 D6
3-U21 D7
OD0
OD1
OD2
OD3
OD4
OD5
OD6
OD7
15-U83
15-U18
BANK 0

FIGURE 14

39

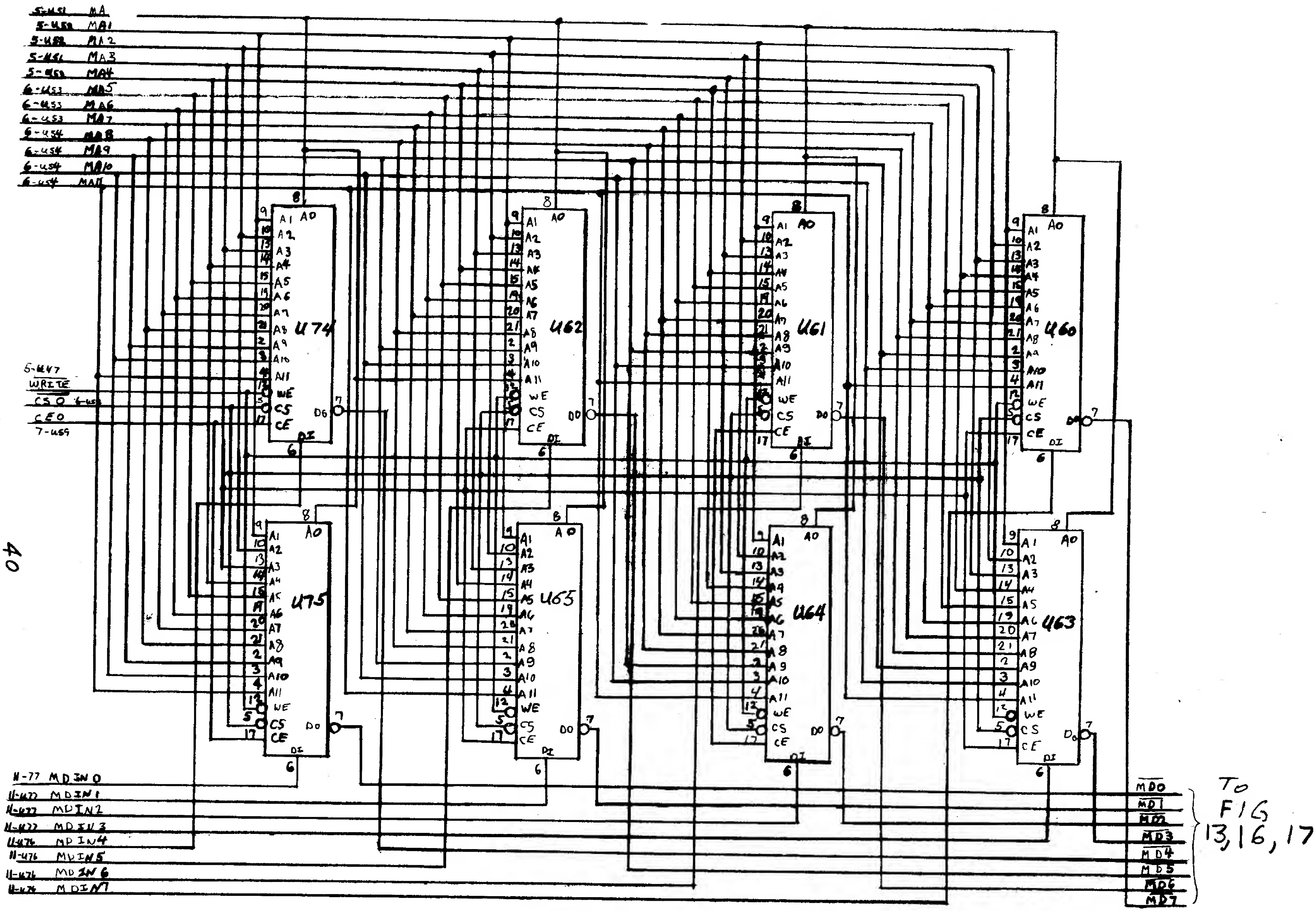


FIGURE 15

BANK 8

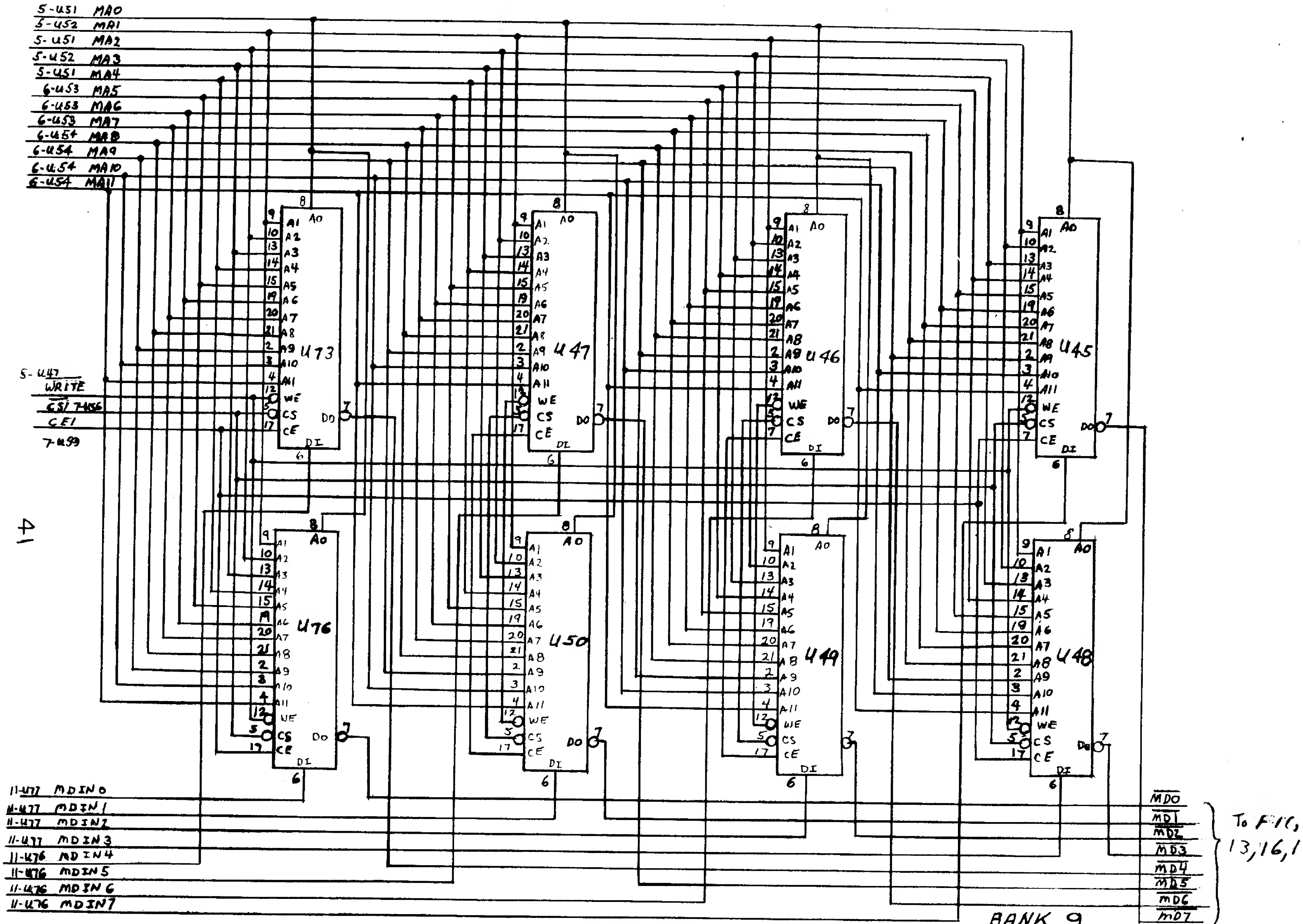
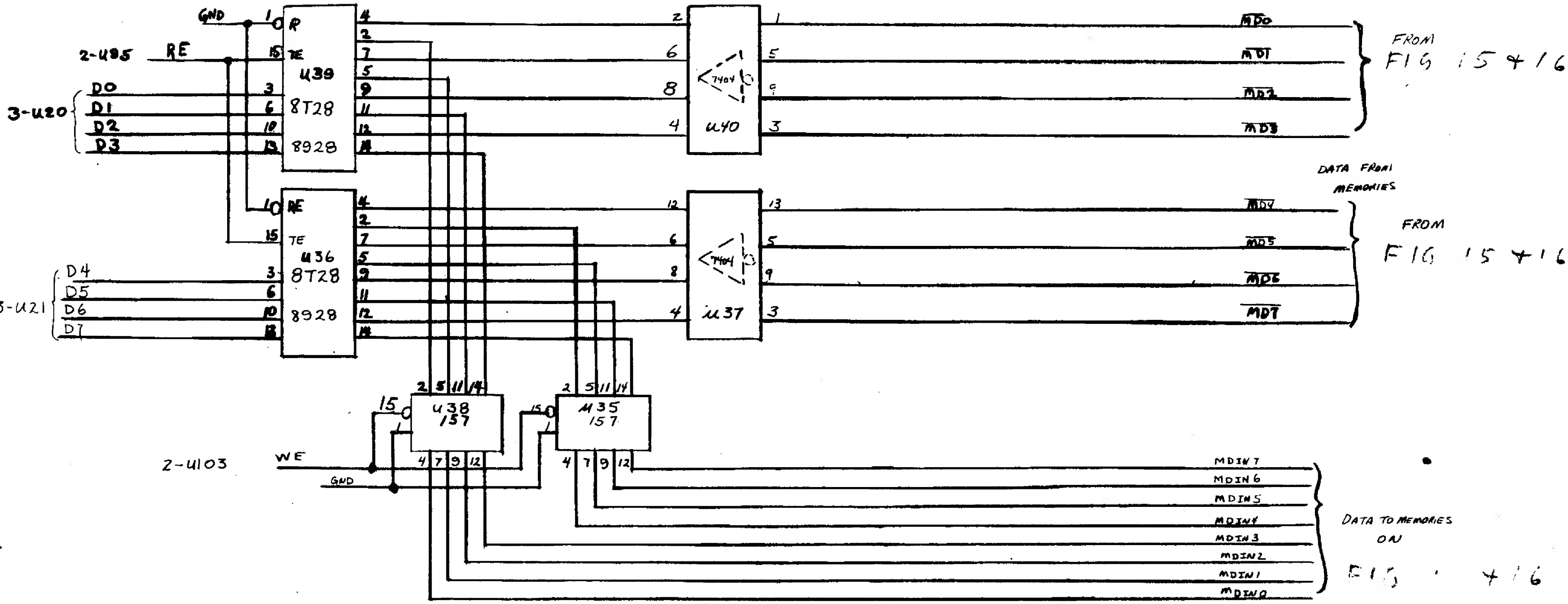

5-U51 MA0
5-U52 MA1
5-U51 MA2
5-U52 MA3
5-U51 MA4
6-U53 MA5
6-U53 MA6
6-U53 MA7
6-U54 MA8
6-U54 MA9
6-U54 MA10
6-U54 MA11
5-U47 WRITE
CS1 7-U56
CE1
7-U59
U73
U47
U46
U45
U76
U50
U49
U48
11-U77 MDIN0
11-U77 MDIN1
11-U77 MDIN2
11-U77 MDIN3
11-U76 MDIN4
11-U76 MDIN5
11-U76 MDIN6
11-U76 MDIN7
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
To FIG, 13, 16, 1
BANK 9

FIGURE 16



INTERFACING

FIGURE 17

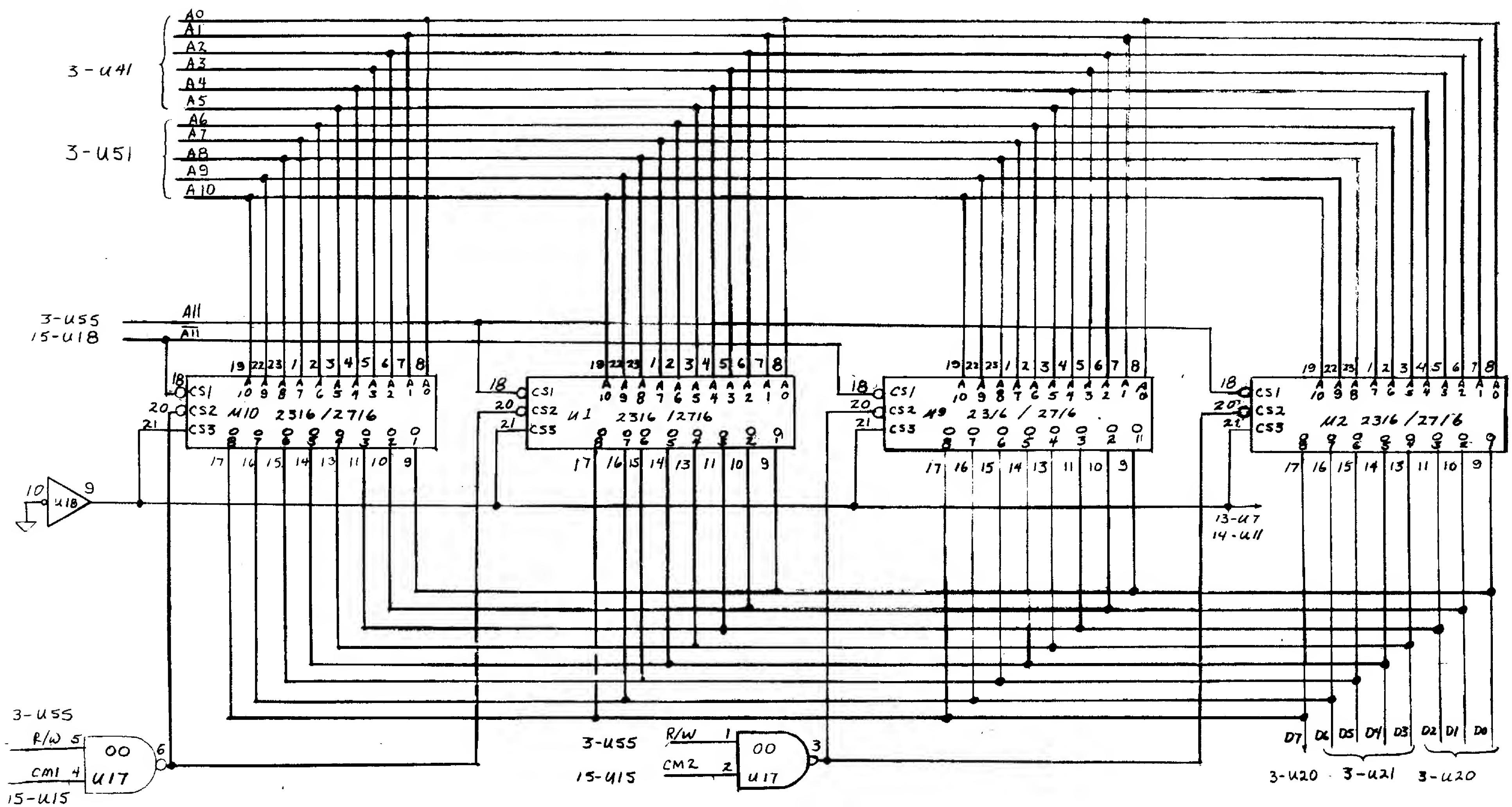
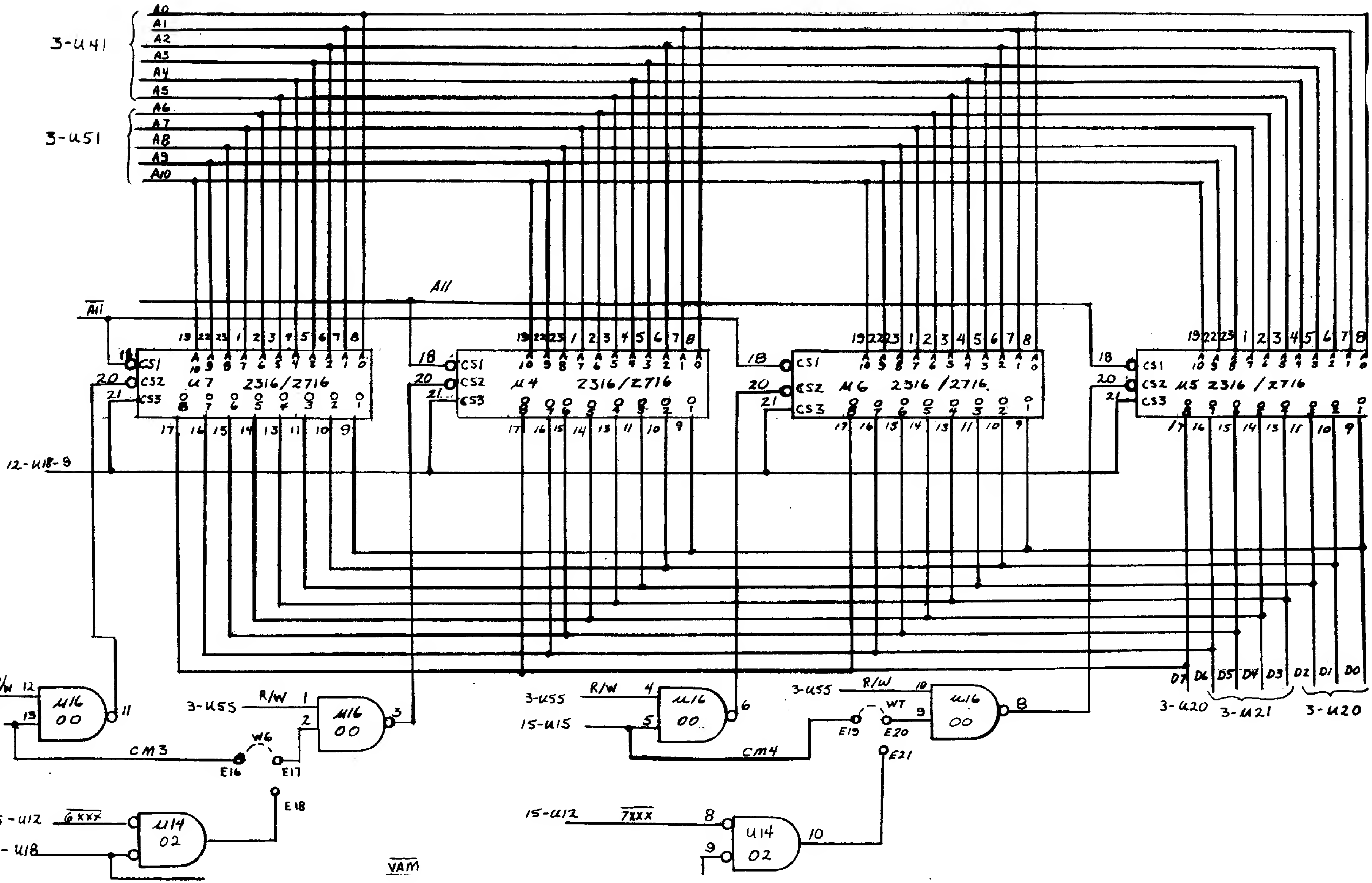


FIGURE 18 ROM ORGANIZATION



3-U41
3-U51
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
U7 2316/2716
U4 2316/2716
U6 2316/2716
U5 2316/2716
CS1
CS2
CS3
12-U18-9
D7 D6 D5 D4 D3 D2 D1 D0
3-U20
3-U21
3-U20
U55 R/W
U15
U16 00
3-U55 R/W
CM3
W6
E16
E17
E18
15-U12 6XXX
15-U18
U14 02
VAM
3-U55 R/W
15-U15
CM4
3-U55 R/W
W7
E19
E20
E21
15-U12 7XXX

FIGURE 19

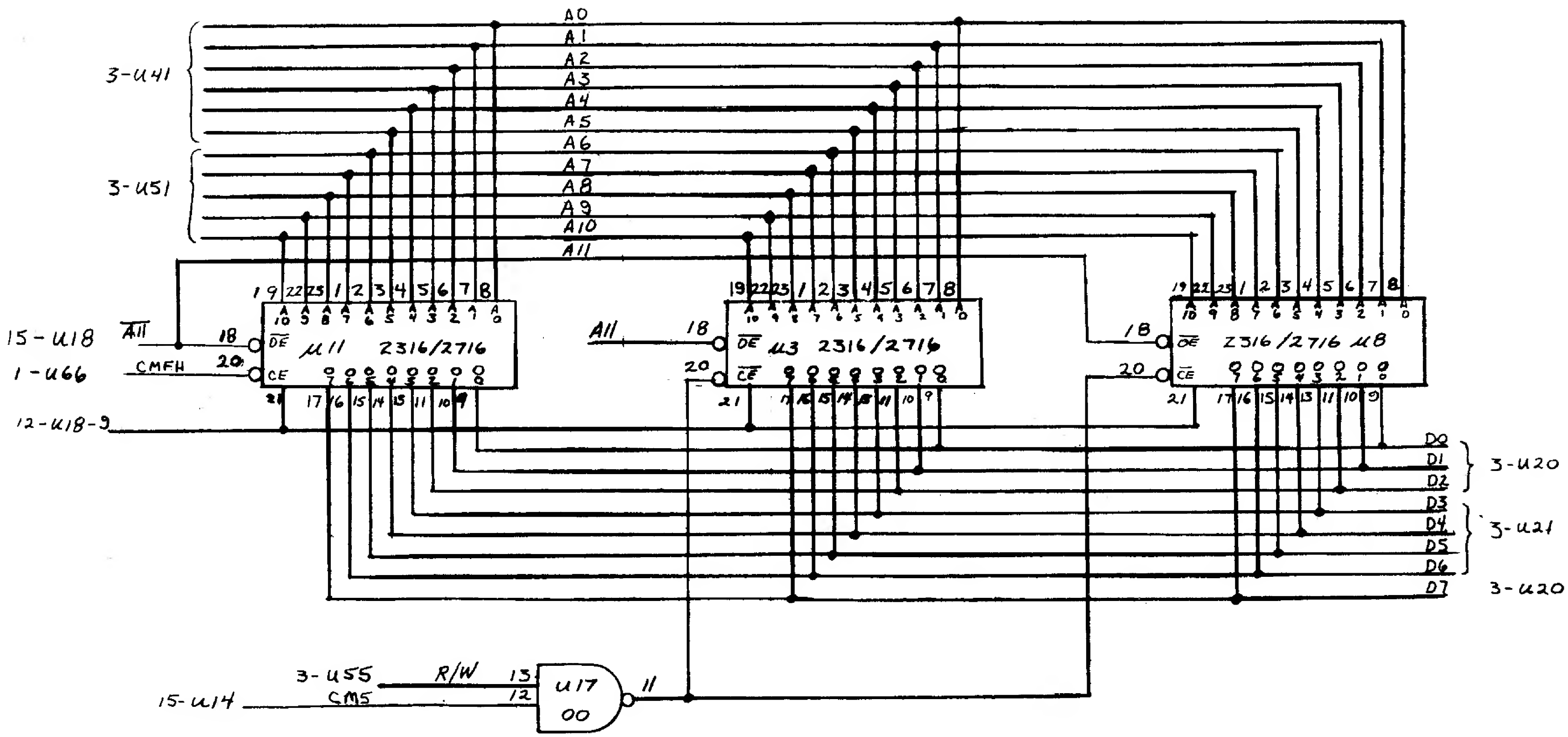

3-U41
3-U51
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
15-U18
1-U66
12-U18-9
CMEH
U11 2316/2716
A11
U3 2316/2716
2316/2716 U8
D0
D1
D2
D3
D4
D5
D6
D7
3-U20
3-U21
3-U20
3-U55
15-U14
R/W
CMS
U17
00

FIGURE 20

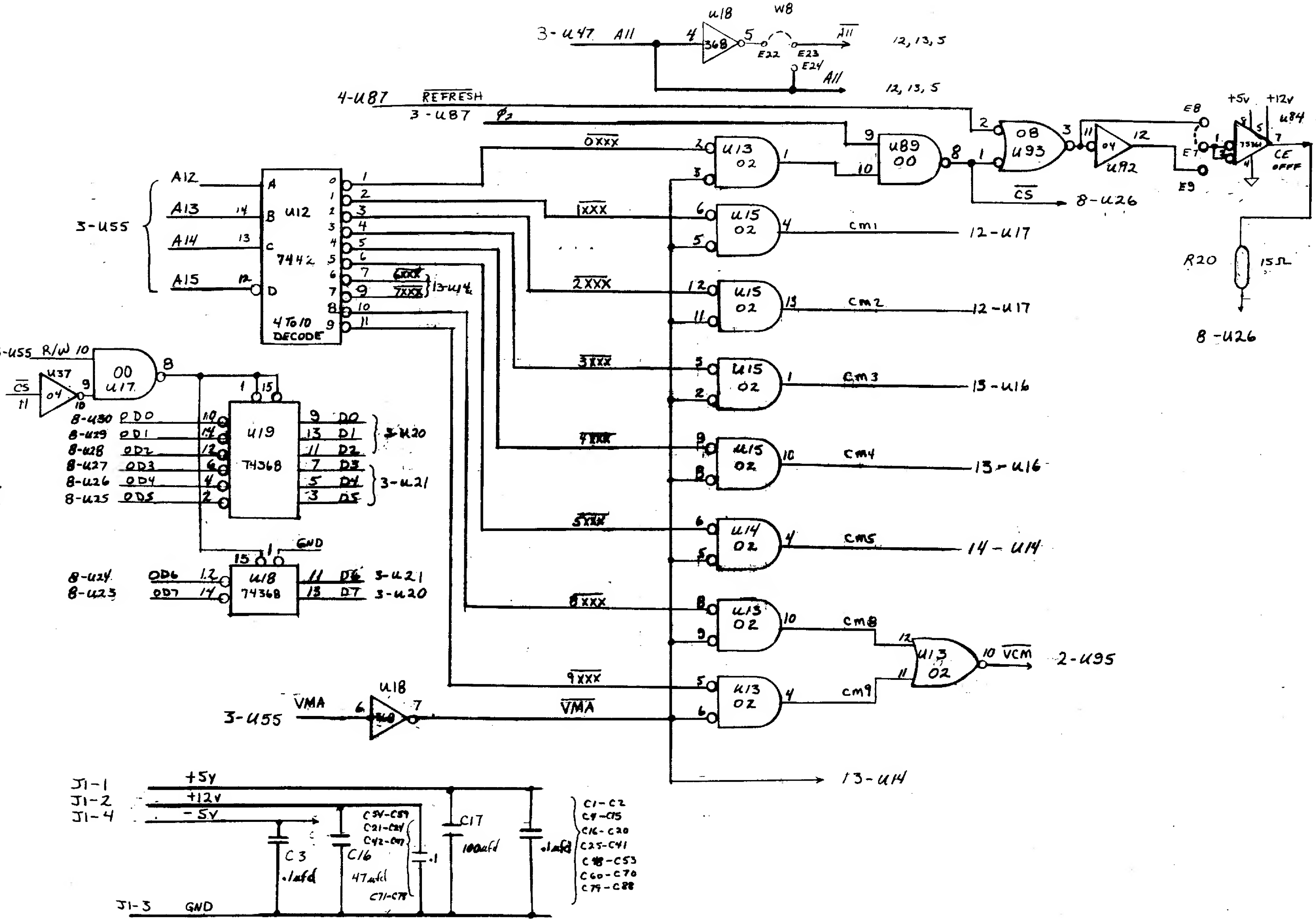
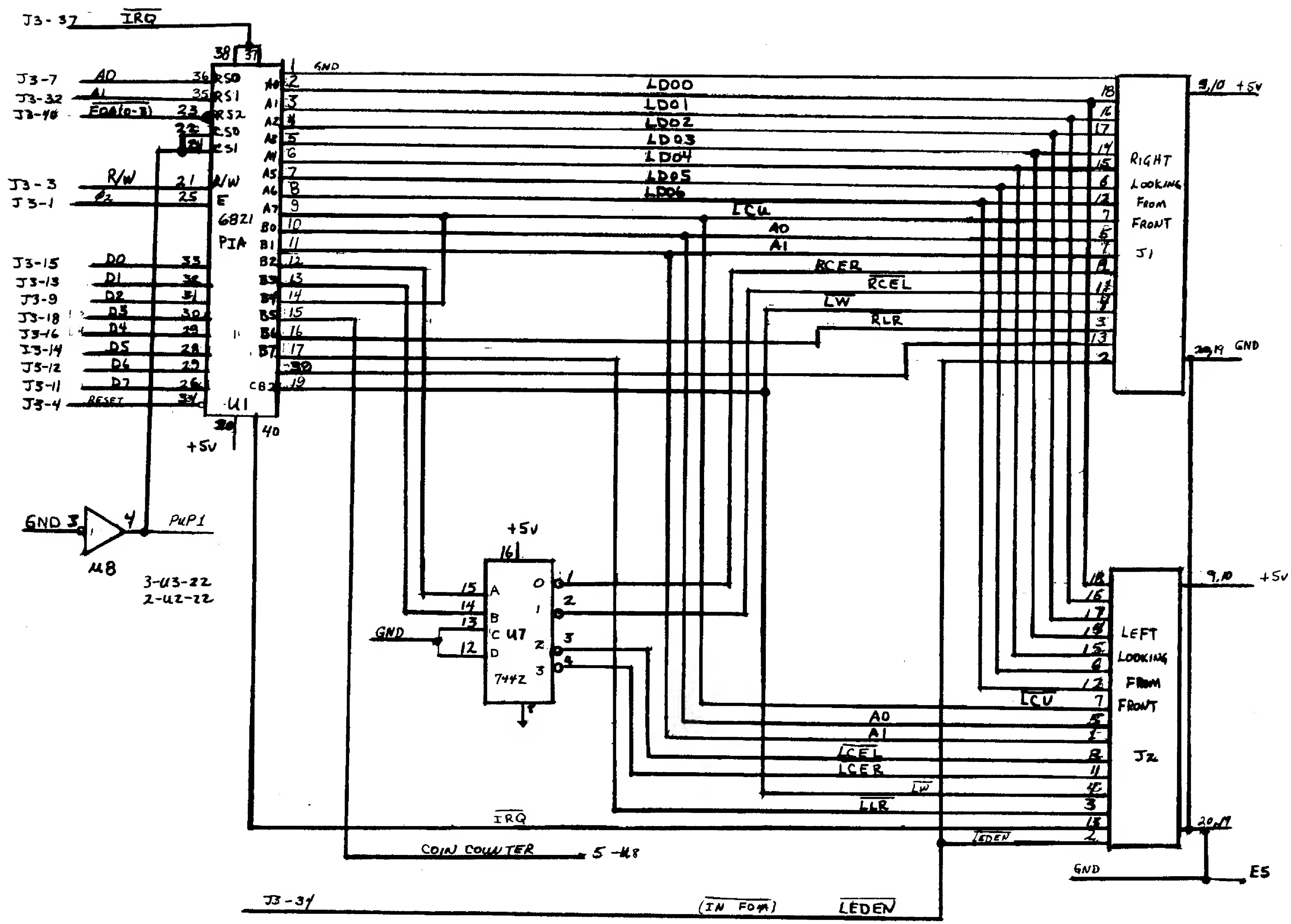

3-U47 A11
U18
368
W8
E22
E23
E24
A11
12, 13, 5
4-U87 REFRESH
3-U87 Φ2
0XXX
1XXX
2XXX
3XXX
4XXX
5XXX
6XXX
7XXX
8XXX
9XXX
13-U14
3-U55
A12
A13
A14
A15
U12
7442
4 To 10
DECODE
U13
02
U89
00
08
U93
04
U92
+5v
+12v
U84
E8
E7
E9
CE
CS
8-U26
U15
CM1
12-U17
CM2
12-U17
CM3
13-U16
CM4
13-U16
U14
CM5
14-U14
CM8
CM9
VCM
2-U95
R20
15Ω
8-U26
3-U55 R/W
00
U17
U37
04
8-U30 ØD0
8-U29 ØD1
8-U28 ØD2
8-U27 ØD3
8-U26 ØD4
8-U25 ØD5
U19
74368
D0
D1
D2
3-U20
D3
D4
D5
3-U21
GND
8-U24 ØD6
8-U23 ØD7
U18
74368
D6 3-U21
D7 3-U20
VMA
3-U55
U18
VMA
13-U14
J1-1 +5v
J1-2 +12v
J1-4 -5v
C3 .1mfd
C16 47mfd
C54-C59
C21-C24
C42-C47
C71-C78
.1
C17 100mfd
.1mfd
C1-C2
C4-C15
C16-C20
C25-C41
C48-C53
C60-C70
C79-C88
J1-3 GND

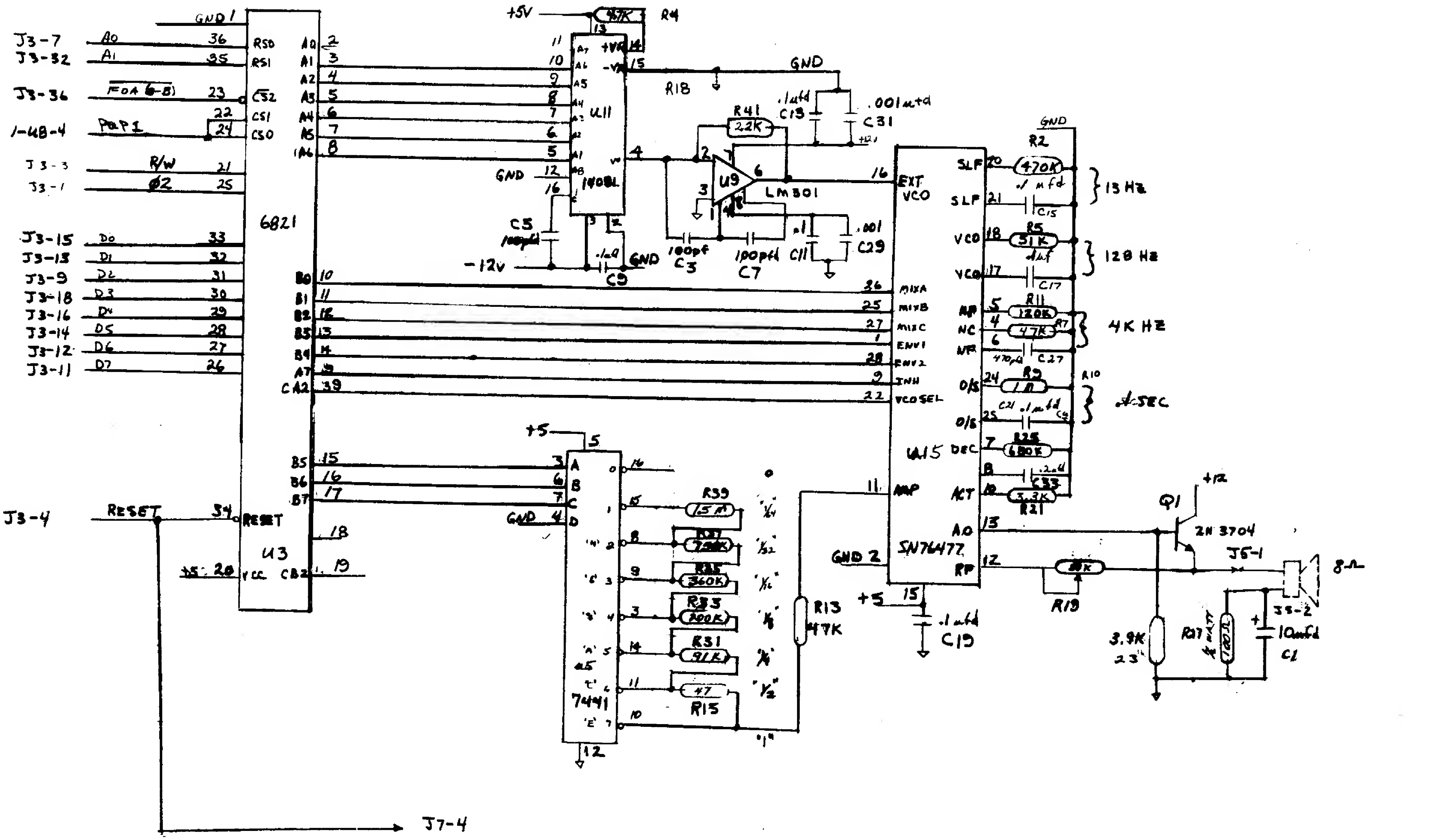
FIGURE 21



BUTTON PIA

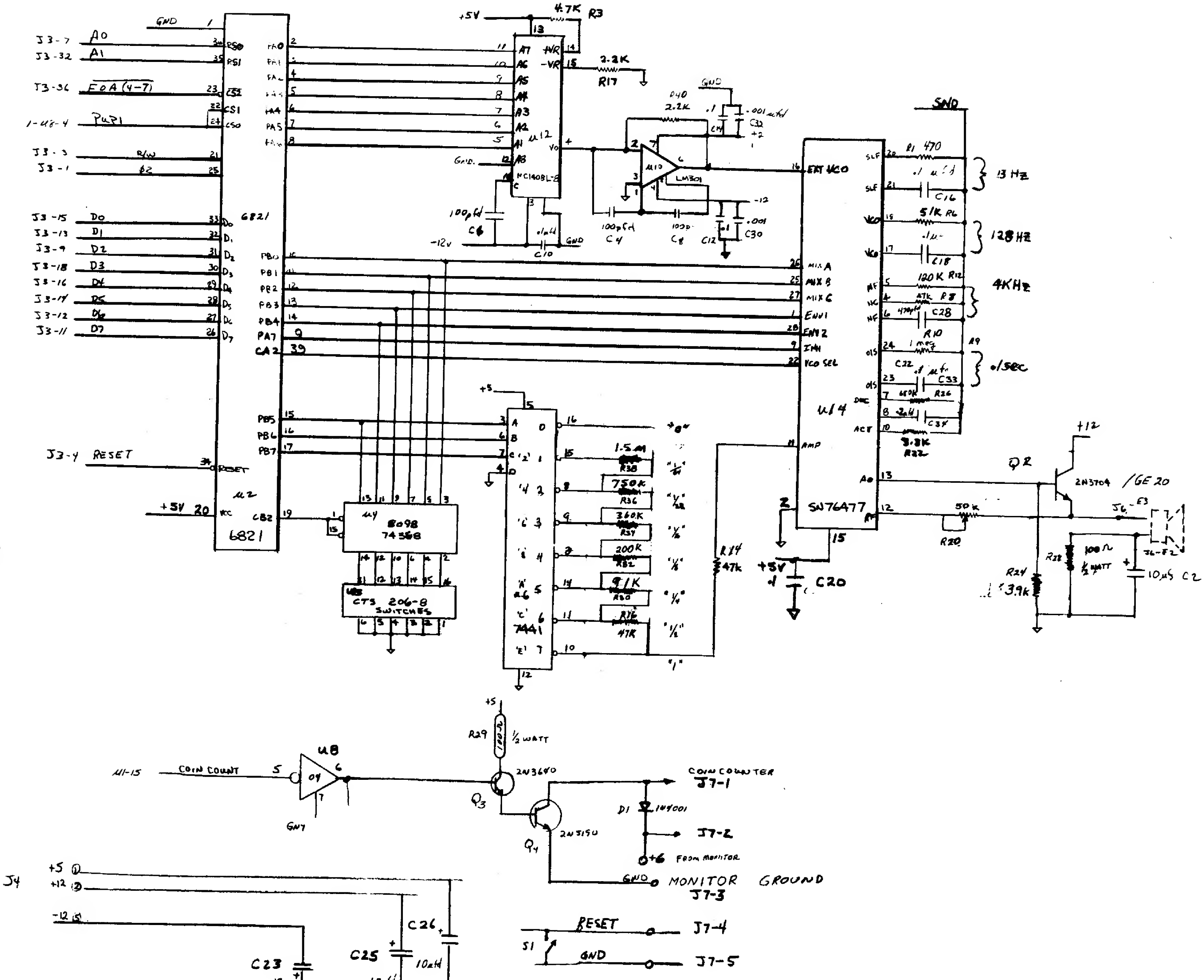
FIGURE 22

47



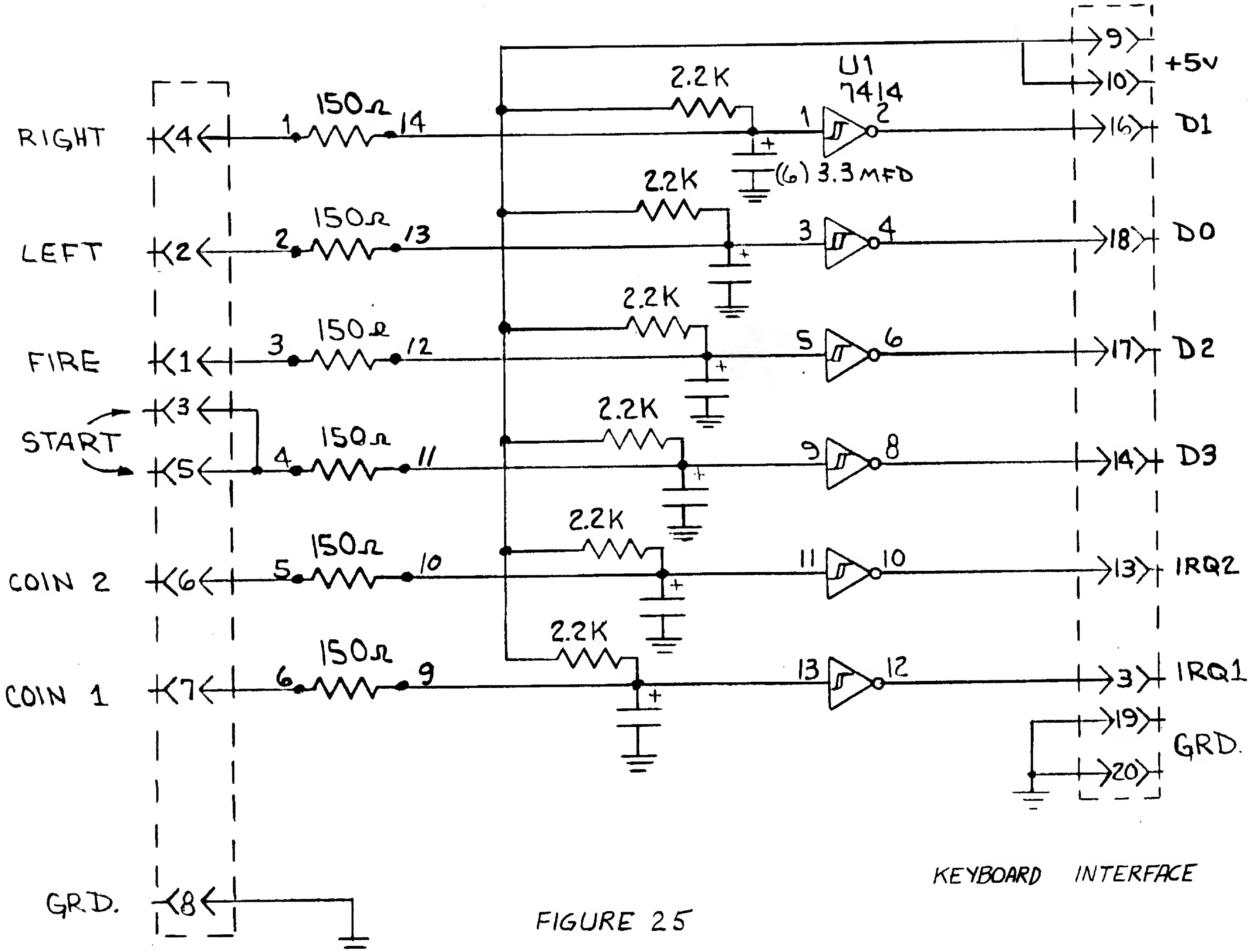
SOUND GENERATOR CONTROL

Figure 23



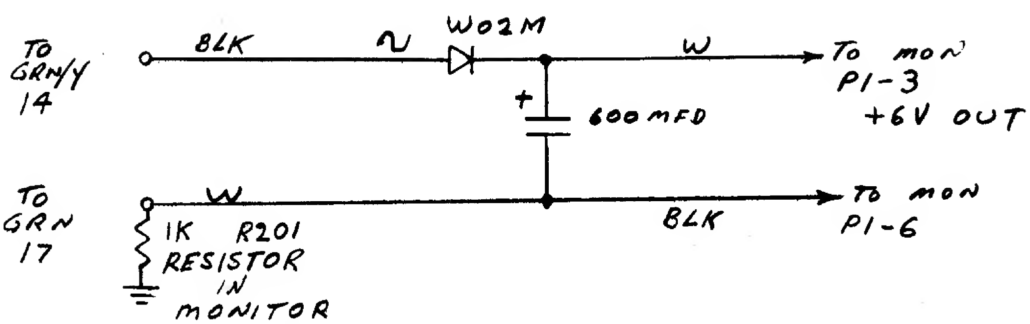
COIN COUNTER CONTROL

FIGURE 24



RIGHT
LEFT
FIRE
START
COIN 2
COIN 1
GRD.
150Ω
2.2K
U1
7414
(6) 3.3 MFD
+5v
D1
D0
D2
D3
IRQ2
IRQ1
GRD.
KEYBOARD INTERFACE

FIGURE 25



6VDC POWERSUPPLY

FIGURE 26

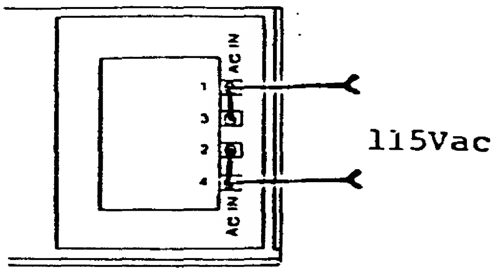
REV. A
8/23/79

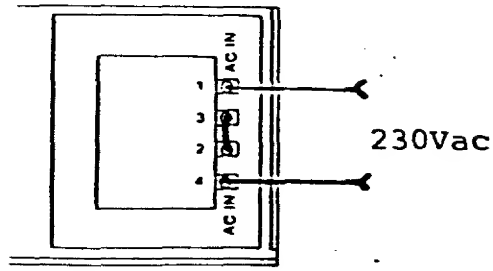
HOOK-UP INSTRUCTIONS FOR LINEAR POWER SUPPLIES

PLT SERIES

Power Input

These units are designed to operate from a nominal 115V or 230V ac (rms). They are shipped with 115V jumpers in place.





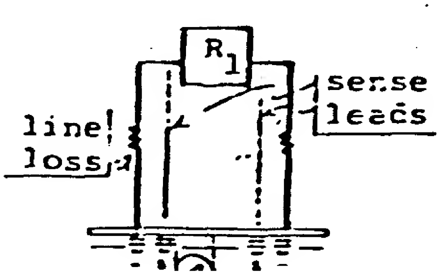
The inputs are isolated from ground, 1500V ac.

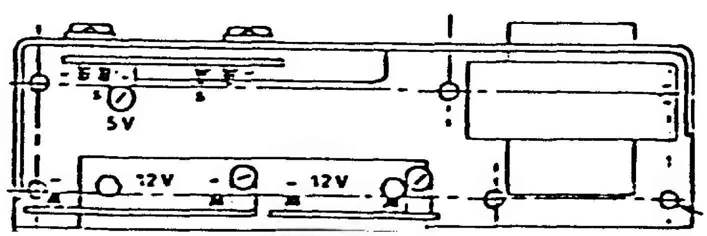
Outputs

All output sections are isolated from each other and from chassis ground, so they can be used as positive or negative supplies, or even "stacked" if desired.

In the PLT series the 12V sections are identical. The (+) terminal is next to the white potentiometer and the (-) terminal is next to the blue pot. In the unlikely event that voltage adjustment is required, turn the white pot slowly while observing the output voltage. (If the voltage is adjusted to maximum, the internal fixed O.V.P. circuit may activate. This will require reducing the pot setting and unplugging the supply to reset.) The blue pot adjusts the "foldback" current. It is not recommended that the user attempt to reset this pot in the field, as damage can result. DAMAGE RESULTING FROM THE BLUE POT ADJUSTMENTS VOIDS WARRANTY.

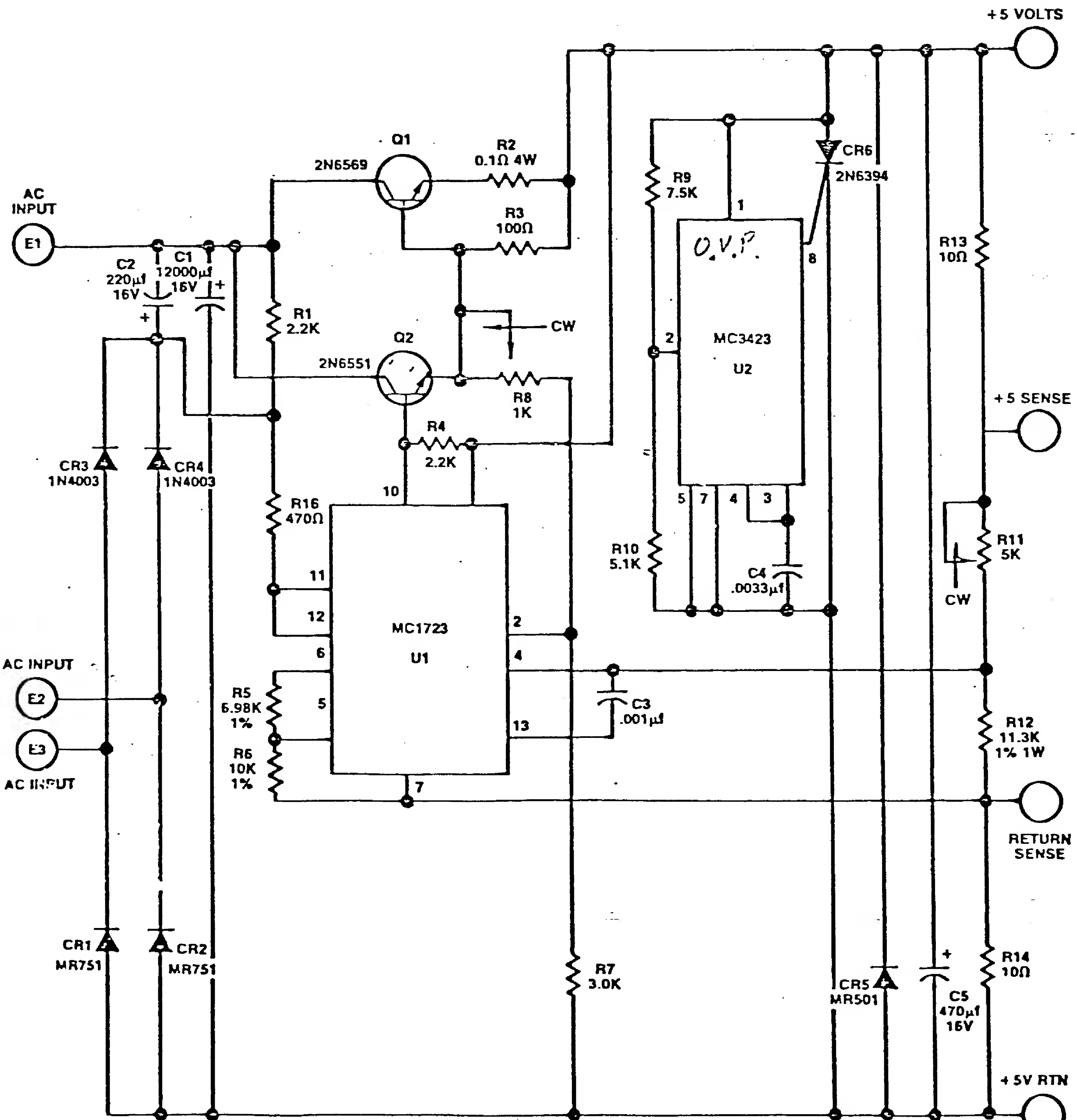
The 5V section is somewhat more elegant, in that a pair of voltage sense terminals are included. These enable the user to overcome up to 0.5V of line drop (total) between the supply and its load. In applications where the load is some distance from the supply, a second pair of wires of lighter gauge can be connected from the sense terminals to the load (carefully observing polarity). In this manner the regulation system can "see" what is happening at the load and control the supply accordingly. BE CAREFUL NOT TO CONNECT ONLY THE SENSE LEADS, WITH THE SUPPLY TURNED ON. DAMAGE WILL RESULT. In applications where line loss is not a problem, it is recommended that the sense terminals be jumpered to the outputs for best regulation.





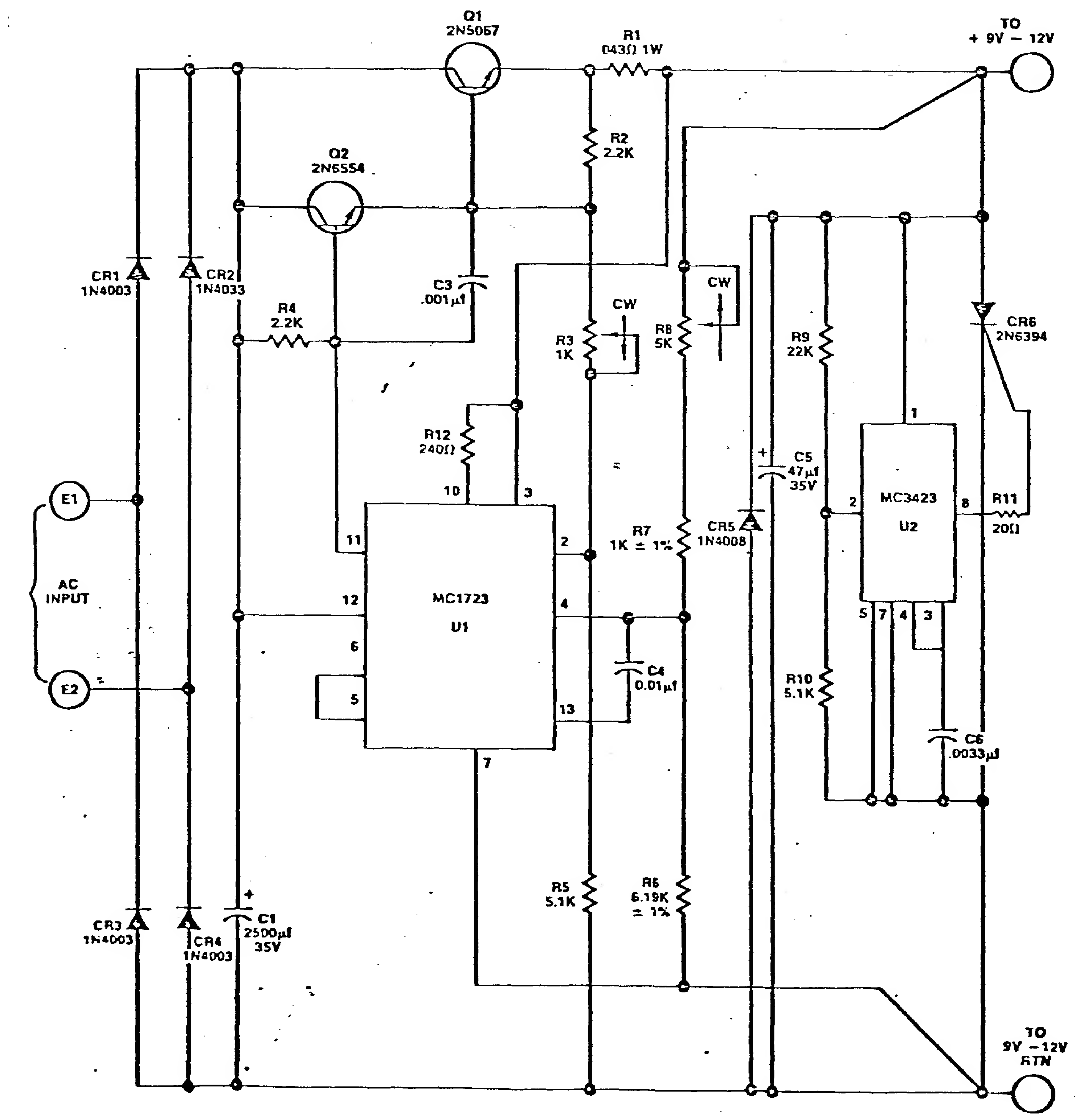
12

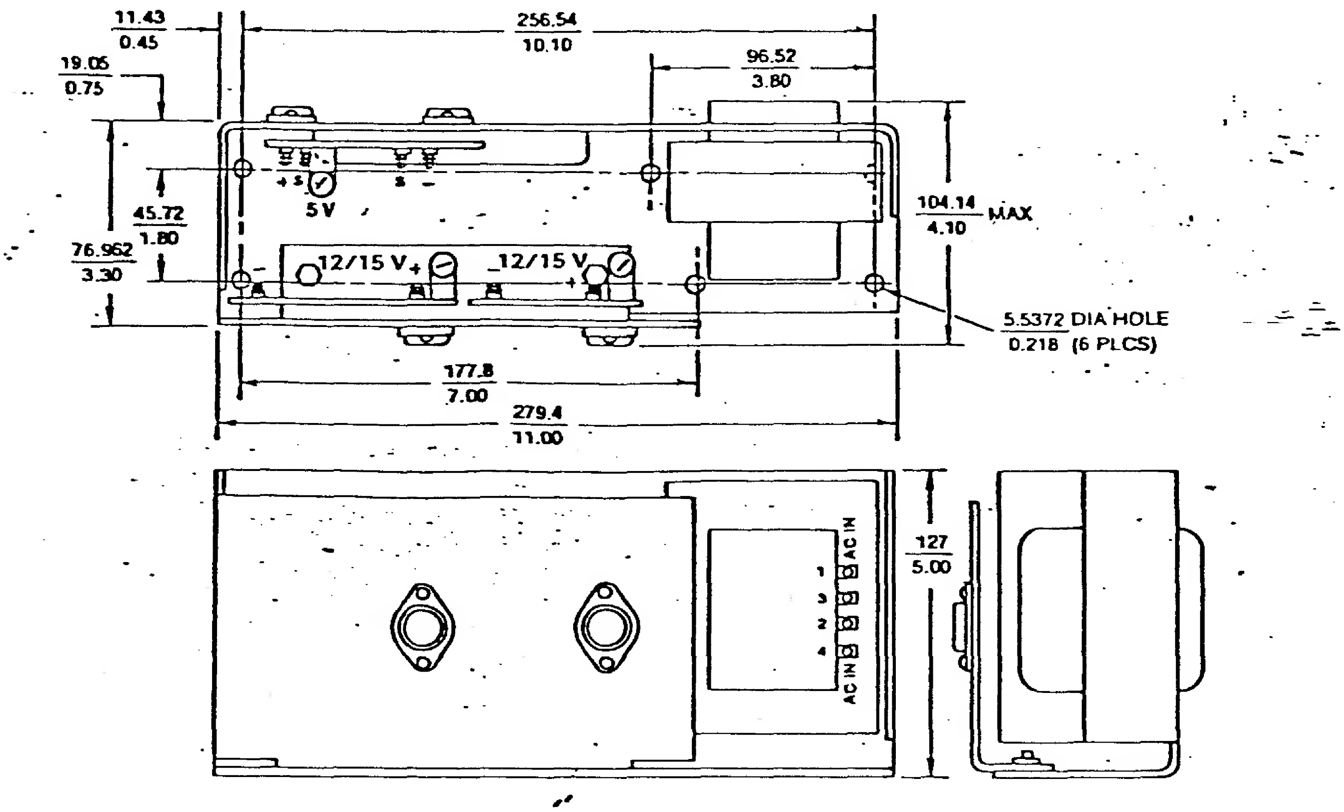
PLT 810 BLOCK DIAGRAM 5 VOLTS



PLT 810

PLT 810 BLOCK DIAGRAM 12 VOLTS ± 4V





Chassis Finish: black anodized

Unit Weights (approx.):
PLT800, 801, 802, 803, 804, 805 — 3.2 lbs. (1.5 kg)
PLT810, 811, 812, 813, 814, 815 — 6.1 lbs. (2.8 kg)
PLT820, 821, 822, 823, 824, 825 — 8.2 lbs. (3.7 kg)

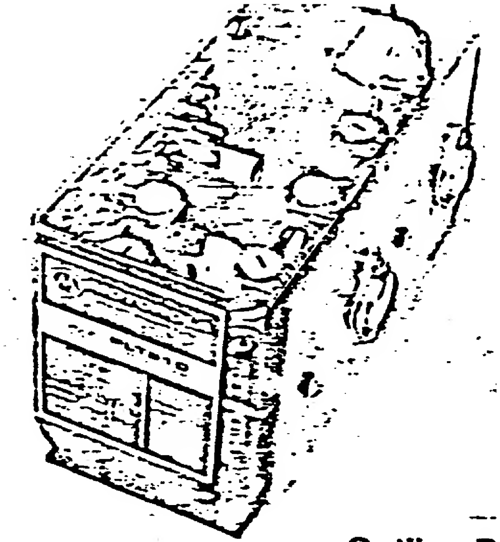
Notes:

All dimensions given in mm/inches.

Terminal and potentiometer locations are relative and not to scale. Voltage adjust potentiometer shown.

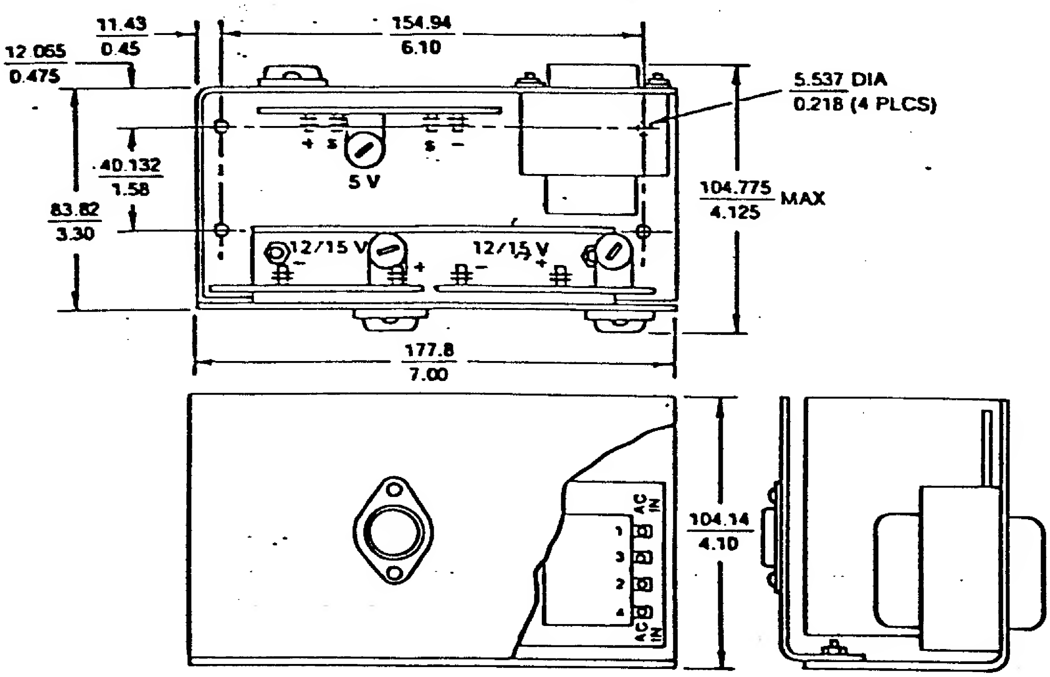
Input	Jumper
115 V	1-3, 2-4
230 V	2-3

Factory connected for 115 V operation.



Outline Drawings

PLT800
thru
PLT805



PLT810
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PLT815